


# HuaQin Confidential

## A5&A21\_M/B Schematics Document

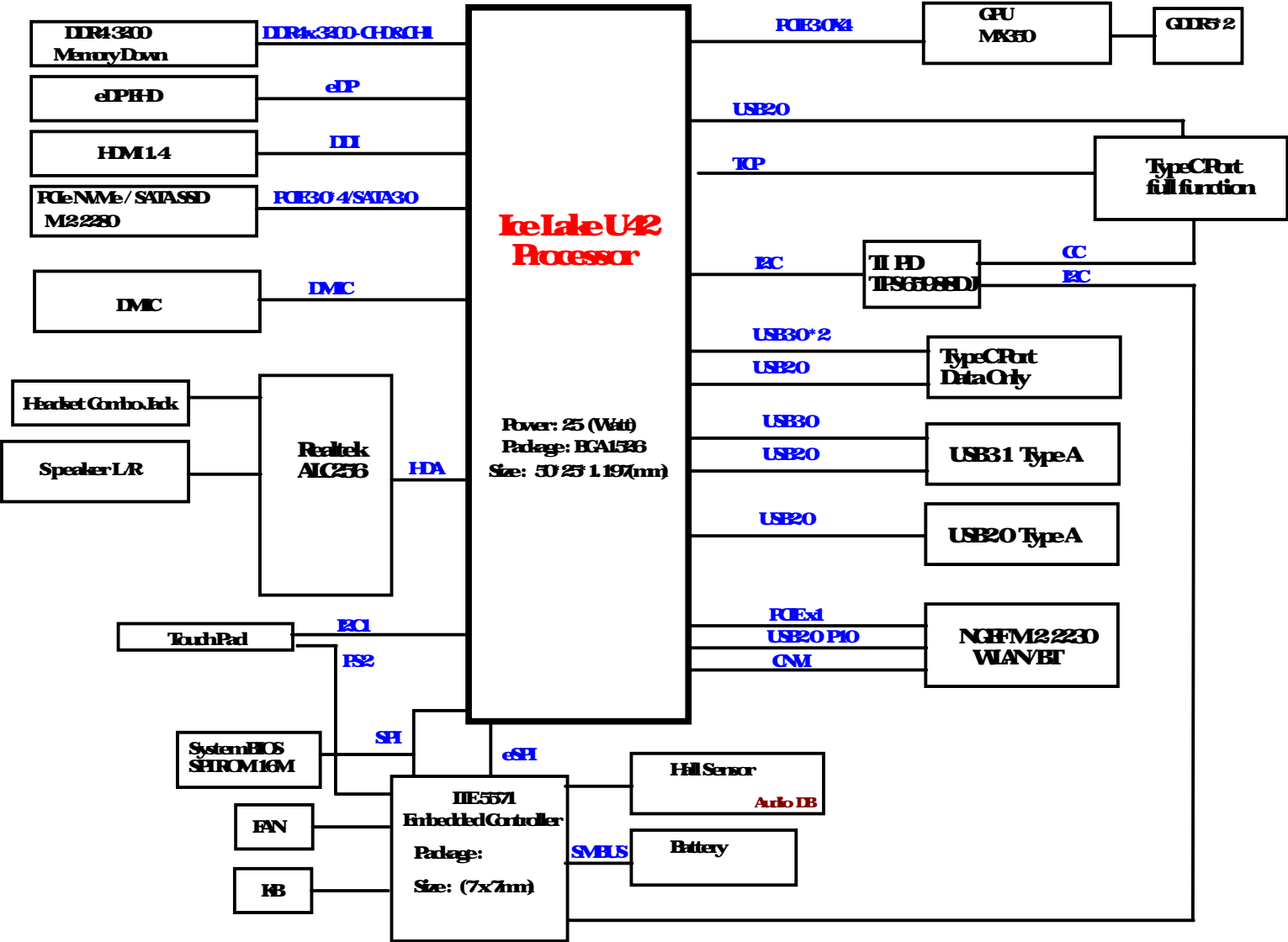
### Intel ICLake U-Processor with DDR4

REV3.0

2020 05 22

 HUAQIN 华勤通信		Huaqin Telecom Technology Co., Ltd	
Page name:		Cover page	
Size: A4	Project Name: A5&A21	REV: V1.0	
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Intel ICL Block Diagram



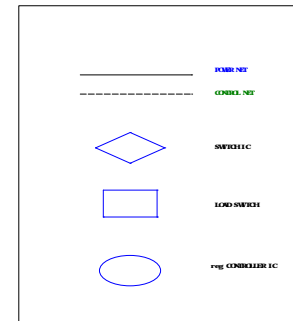
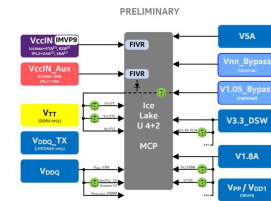
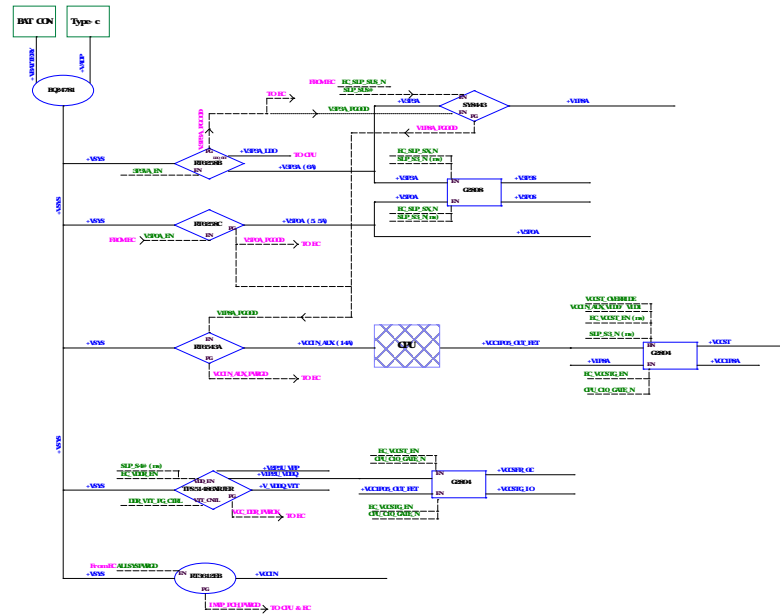
MEMID

HWID0	HWID1	HWID2	HWID3	HWID4	HWID5		Description	Total
0	0	0	0	0	0		SAM8G K4A8G165WE BCM	
1	0	0	0	0	0		MC 8G M9D0A512M6IB 082E J	
0	1	0	0	0	0		SAM16G K4A8G165WA BCM	
1	1	0	0	0	0		MC 16G M9D0A1G16RD 082E E	

TBT

HWID3	Description
1	W/TBT
0	W' TBT

## A5&A21 POWER MAP



```
G3 SS FOUR UP FLOW
RIC --> RICSTG --> V3P8A --> V3P8A_PUMCD --> V5P0A --> V5P0A_PUMCD --> DSW/PUMCD --> V1P8A --> V1P8A_PUMCD --> VCCIN/ALX --> VCCIN/ALX_PUMCD --> FSNMIS#
SS SO FOUR UP FLOW
VCCST --> VCCSTG --> VDDQ --> VCCPLCC --> (Other main power) --> VCCIN
```

### Power On Sequence Diagram

**AG IN Mode**

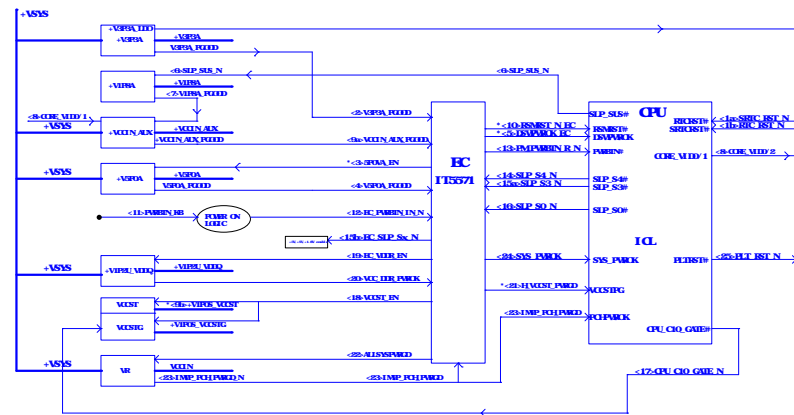
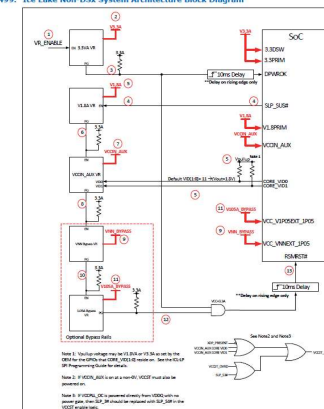
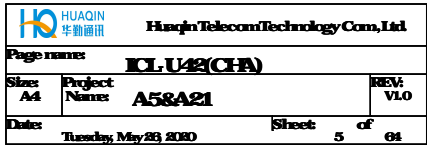


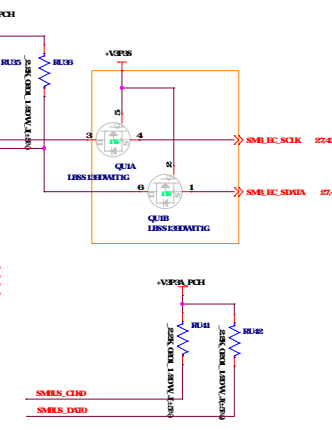
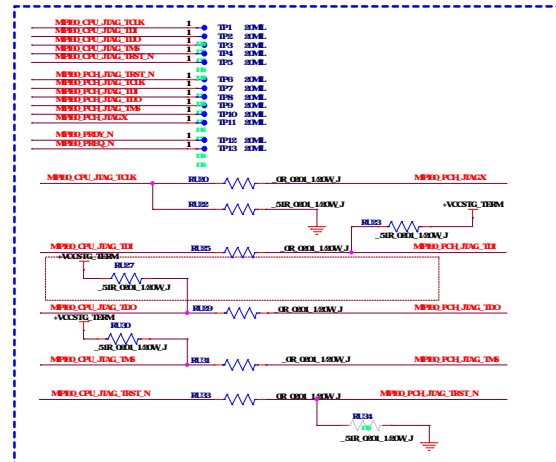
Figure 499. Ice Lake Non-DSx System Architecture Block Diagram





		UUC		???		
BYTE0	23	MB.DQ.0	AK28	DDRC.DQ0.0DDR1.DQ0.0	Y48	MB.CK.DDRO.DN
	23	MB.DQ.1	AK25	DDRC.DQ0.1DDR1.DQ0.1	Y47	MB.CK.DDRO.DP
	23	MB.DQ.2	AK29	DDRC.DQ0.2DDR1.DQ0.2	M3	MB.CK.DDRO.DP
	23	MB.DQ.3	AK27	DDRC.DQ0.3DDR1.DQ0.3	M2	
	23	MB.DQ.4	AK25	DDRC.DQ0.4DDR1.DQ0.4	U45	MB.CK80
	23	MB.DQ.5	AK28	DDRC.DQ0.5DDR1.DQ0.5	V46	MB.CK80
	23	MB.DQ.6	AK29	DDRC.DQ0.6DDR1.DQ0.6	M1	
	23	MB.DQ.7	AK28	DDRC.DQ0.7DDR1.DQ0.7	P43	
BYTE1	23	MB.DQ.8	AL30	DDRC.DQ1.0DDR1.DQ1.0	V42	MB.CS0.N
	23	MB.DQ.9	AK29	DDRC.DQ1.1DDR1.DQ1.1	V39	MB.CS0.N
	23	MB.DQ.10	AL23	DDRC.DQ1.2DDR1.DQ1.2	Y39	
	23	MB.DQ.11	AL28	DDRC.DQ1.3DDR1.DQ1.3	T39	
	23	MB.DQ.12	AL22	DDRC.DQ1.4DDR1.DQ1.4	T38	MB.BA0
	23	MB.DQ.13	AL22	DDRC.DQ1.5DDR1.DQ1.5	T42	MB.BA1
	23	MB.DQ.14	AL23	DDRC.DQ1.6DDR1.DQ1.6	R45	MB.BG0
	23	MB.DQ.15	AL23	DDRC.DQ1.7DDR1.DQ1.7	N47	MB.BG1
BYTE2	23	MB.DQ.16	AB49	DDRC.DQ2.0DDR1.DQ2.0	M2	MB.MA.0
	23	MB.DQ.17	AB48	DDRC.DQ2.1DDR1.DQ2.1	Y49	MB.MA.1
	23	MB.DQ.18	AE49	DDRC.DQ2.2DDR1.DQ2.2	U48	MB.MA.2
	23	MB.DQ.19	AE47	DDRC.DQ2.3DDR1.DQ2.3	Y45	MB.MA.3
	23	MB.DQ.20	AB47	DDRC.DQ2.4DDR1.DQ2.4	U47	MB.MA.4
	23	MB.DQ.21	AB45	DDRC.DQ2.5DDR1.DQ2.5	R49	MB.MA.5
	23	MB.DQ.22	AE45	DDRC.DQ2.6DDR1.DQ2.6	U49	MB.MA.6
	23	MB.DQ.23	AD38	DDRC.DQ2.7DDR1.DQ2.7	M7	MB.MA.7
BYTE3	23	MB.DQ.24	AD39	DDRC.DQ3.0DDR1.DQ3.0	M5	MB.MA.8
	23	MB.DQ.25	AE39	DDRC.DQ3.1DDR1.DQ3.1	R47	MB.MA.9
	23	MB.DQ.26	AE43	DDRC.DQ3.2DDR1.DQ3.2	F39	MB.MA.10
	23	MB.DQ.27	AE38	DDRC.DQ3.3DDR1.DQ3.3	N48	MB.MA.11
	23	MB.DQ.28	AD43	DDRC.DQ3.4DDR1.DQ3.4	R48	MB.MA.12
	23	MB.DQ.29	AD42	DDRC.DQ3.5DDR1.DQ3.5	Y41	MB.MA.13
	23	MB.DQ.30	AE42	DDRC.DQ3.6DDR1.DQ3.6	V41	MB.MA.14
	23	MB.DQ.31	J48	DDRC.DQ3.7DDR1.DQ3.7	Y42	MB.MA.15
BYTE4	24	MB.DQ.32	J45	DDRD.DQ0.0DDR1.DQ4.0	V47	MB.MA.16
	24	MB.DQ.33	J49	DDRD.DQ0.1DDR1.DQ4.1	V43	MB.CDI0
	24	MB.DQ.34	G47	DDRD.DQ0.2DDR1.DQ4.2	V38	
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BYTE5	24	MB.DQ.40	G39	DDRD.DQ1.0DDR1.DQ5.0	AE41	MB.DQS.2.DP
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BYTE6	24	MB.DQ.48	D43	DDRD.DQ2.0DDR1.DQ6.0	D43	MB.DQS.6.DP
	24	MB.DQ.49	A43	DDRD.DQ2.1DDR1.DQ6.1	C36	MB.DQS.7.DN
	24	MB.DQ.50	C40	DDRD.DQ2.2DDR1.DQ6.2	M38	MB.PARITY
	24	MB.DQ.51	C43	DDRD.DQ2.3DDR1.DQ6.3	M40	MB.ACT.N
	24	MB.DQ.52	D40	DDRD.DQ2.4DDR1.DQ6.4	M40	MB.ALER.N
	24	MB.DQ.53	B40	DDRD.DQ2.5DDR1.DQ6.5		
	24	MB.DQ.54	A40	DDRD.DQ2.6DDR1.DQ6.6		
	24	MB.DQ.55	E45	DDRD.DQ2.7DDR1.DQ6.7		
BYTE7	24	MB.DQ.56	D45	DDRD.DQ3.0DDR1.DQ7.0		
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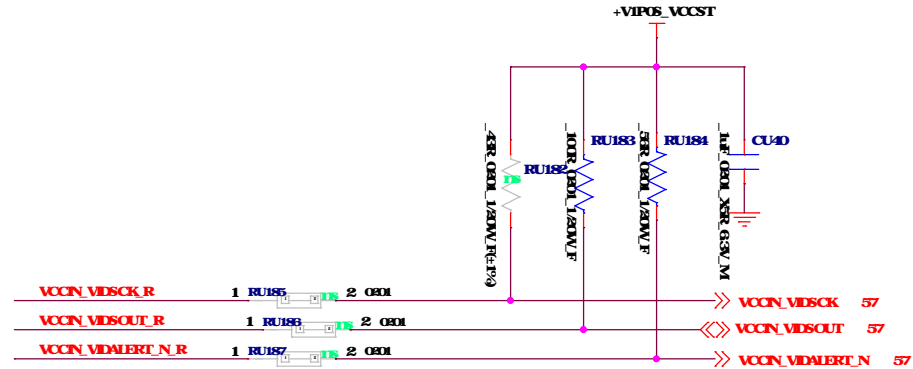
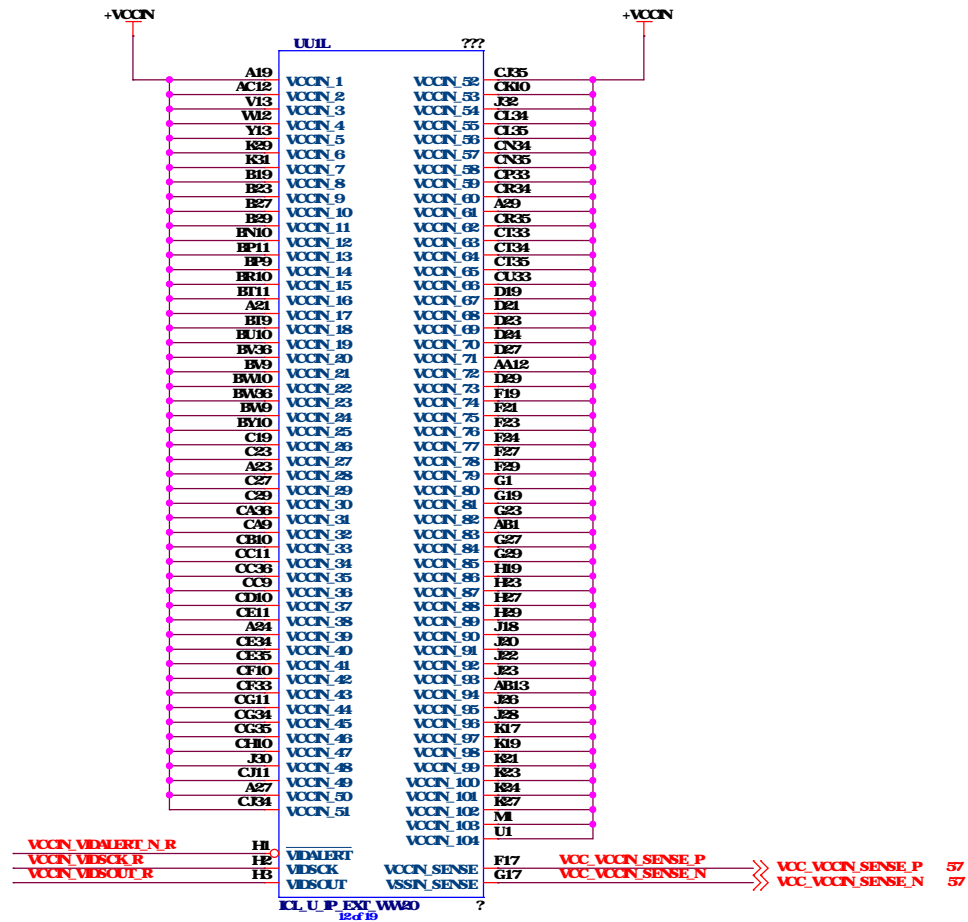








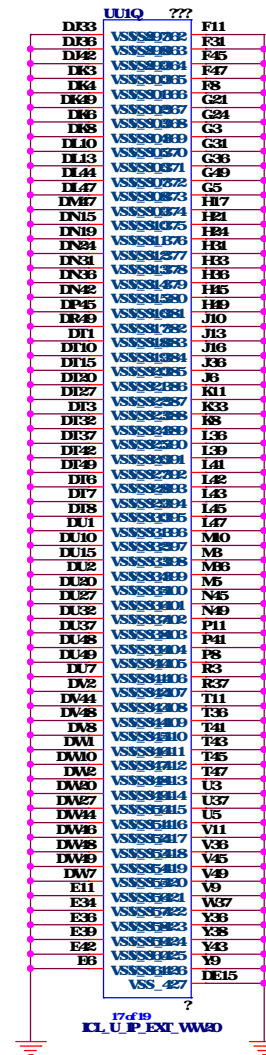
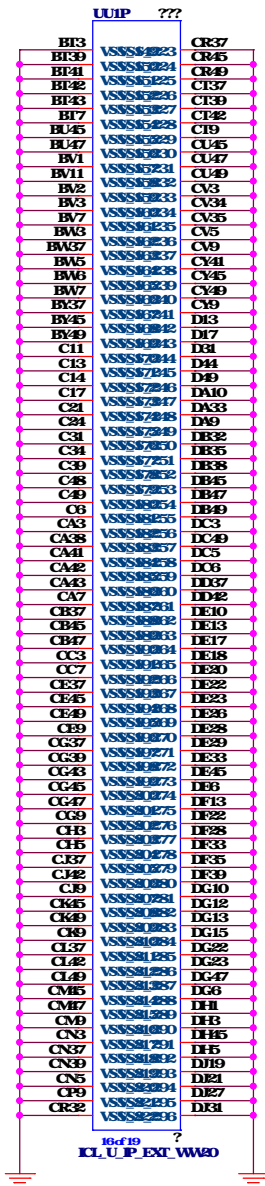
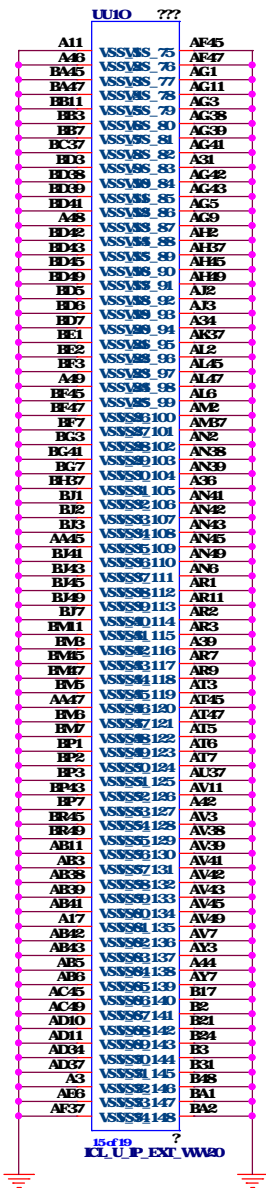




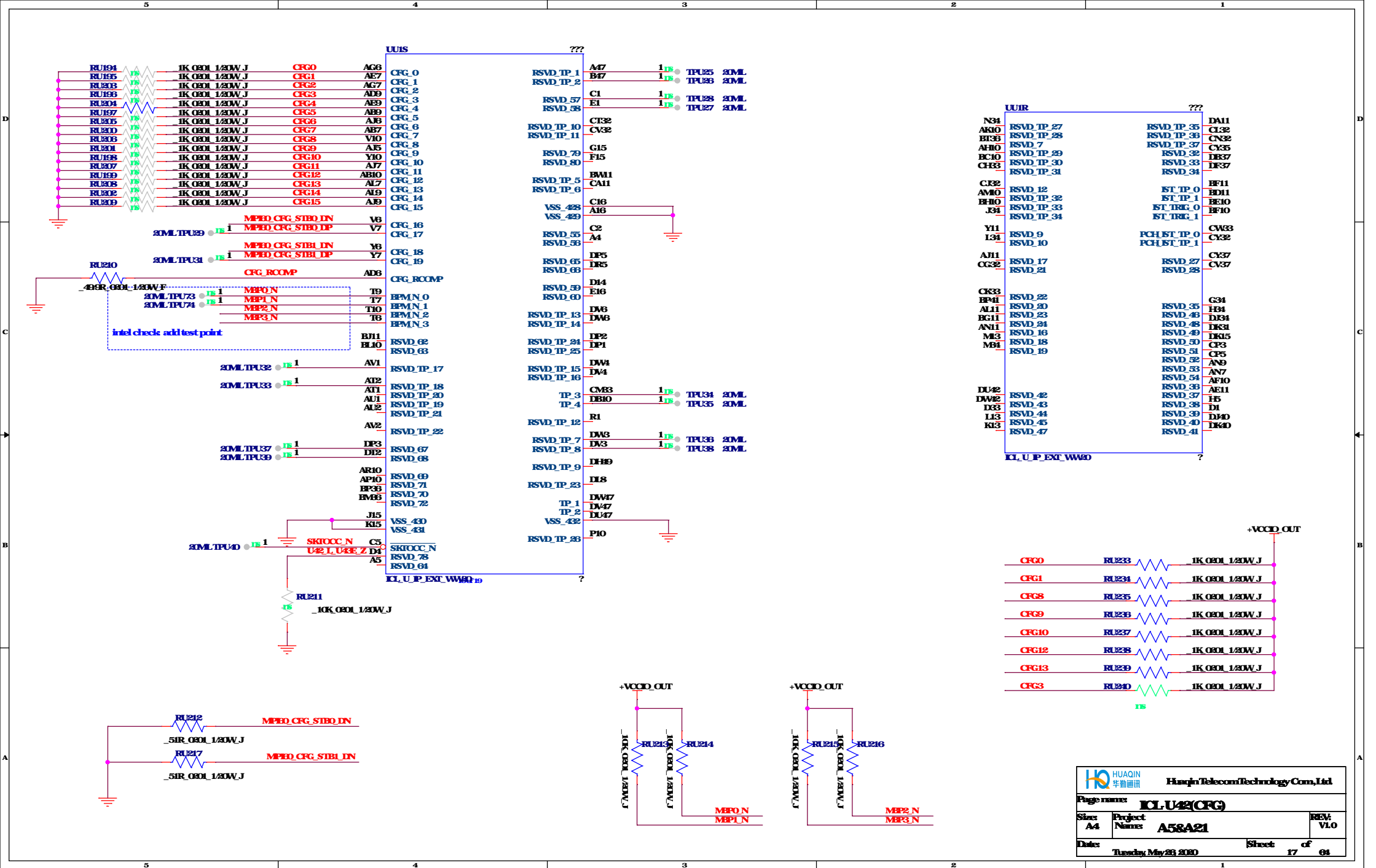


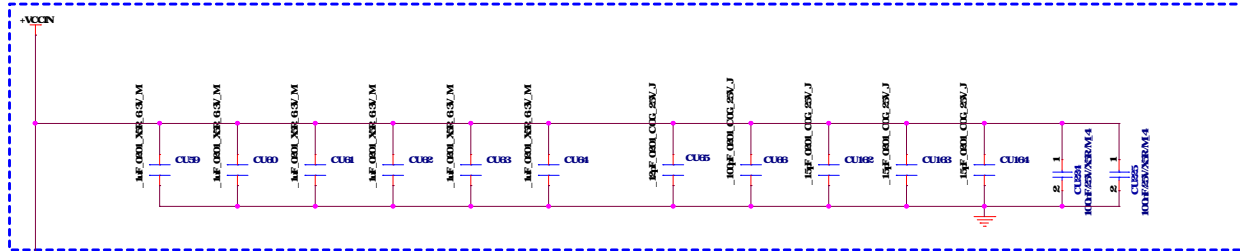




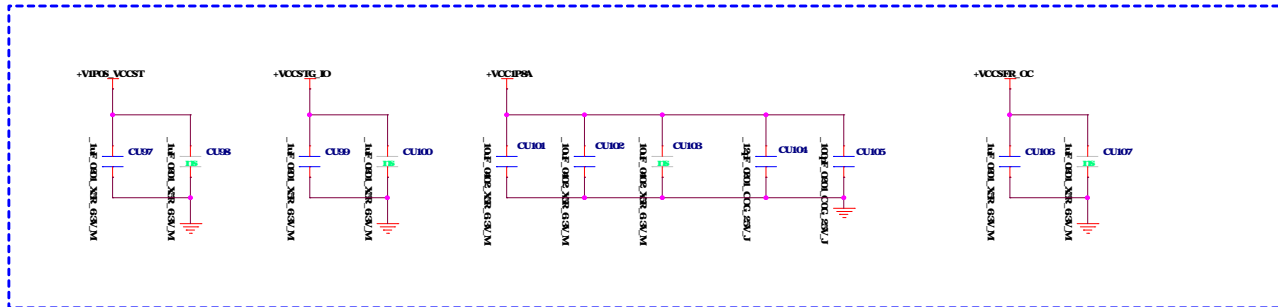
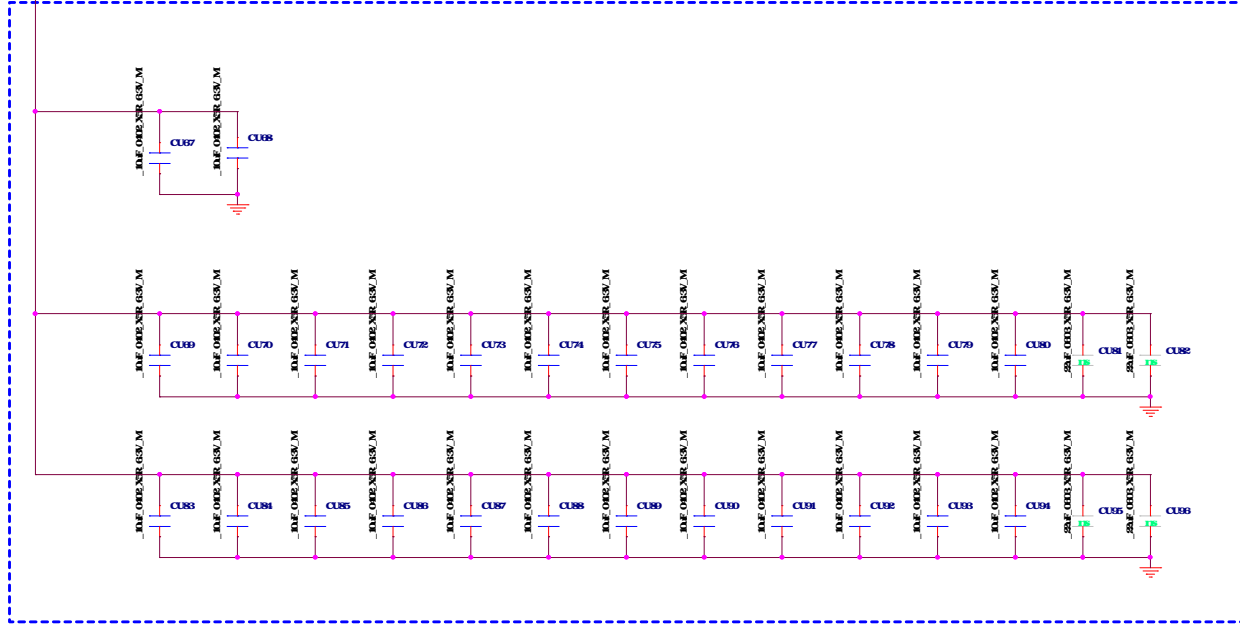


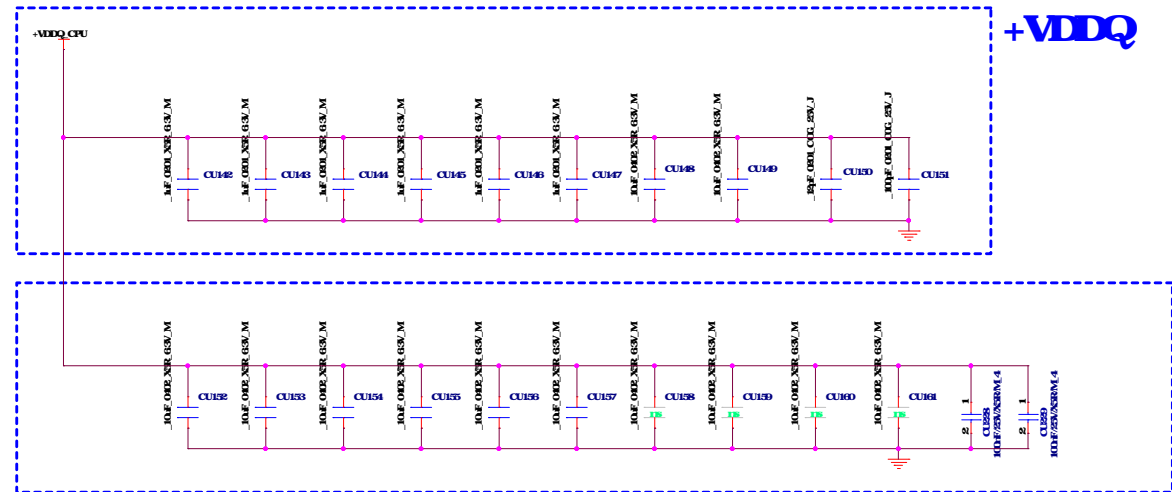
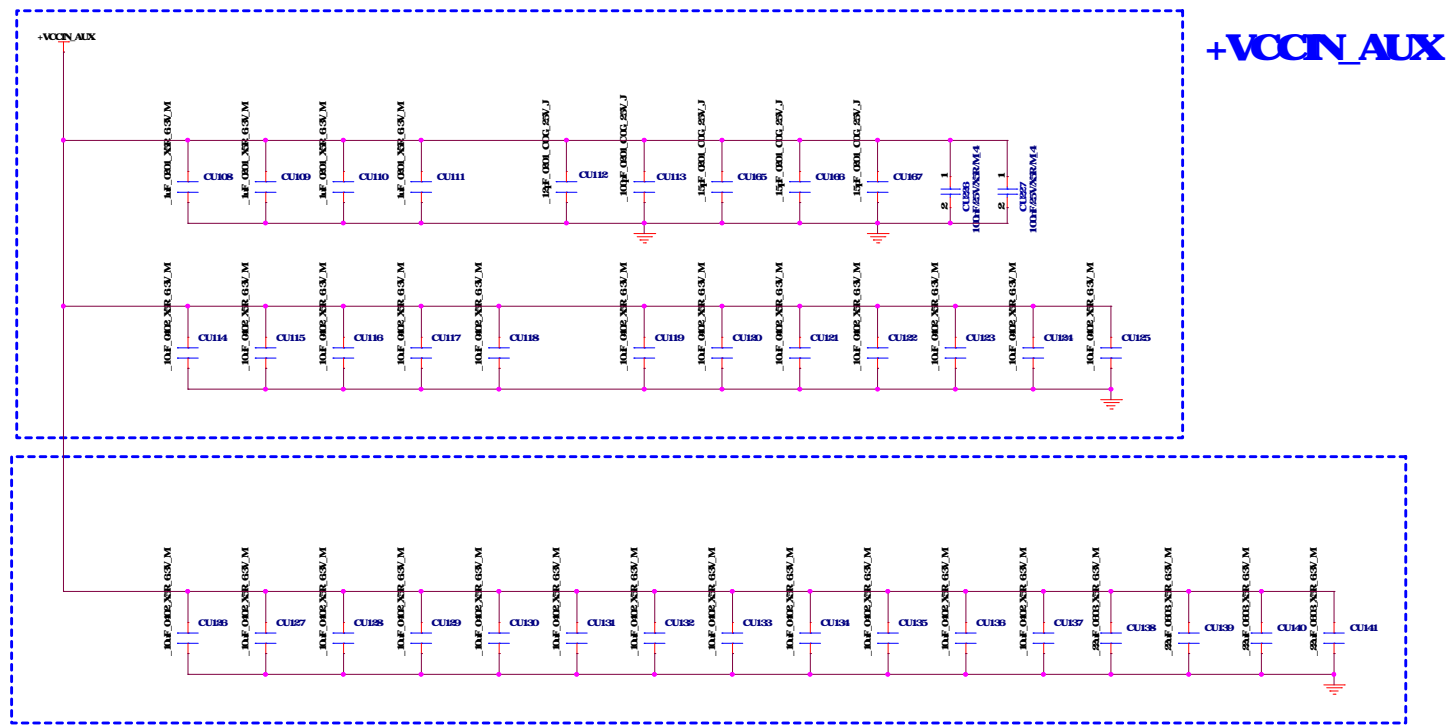


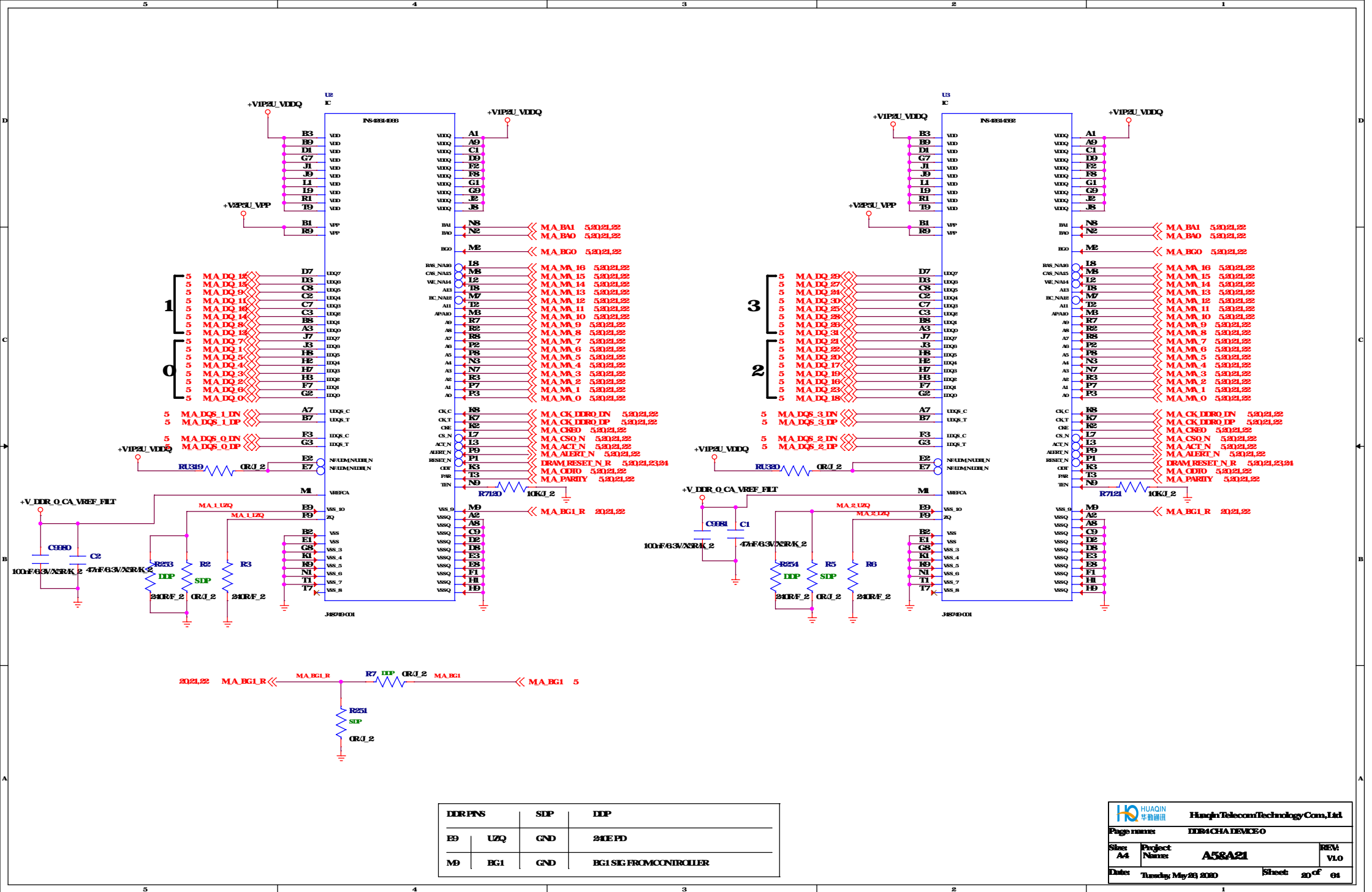




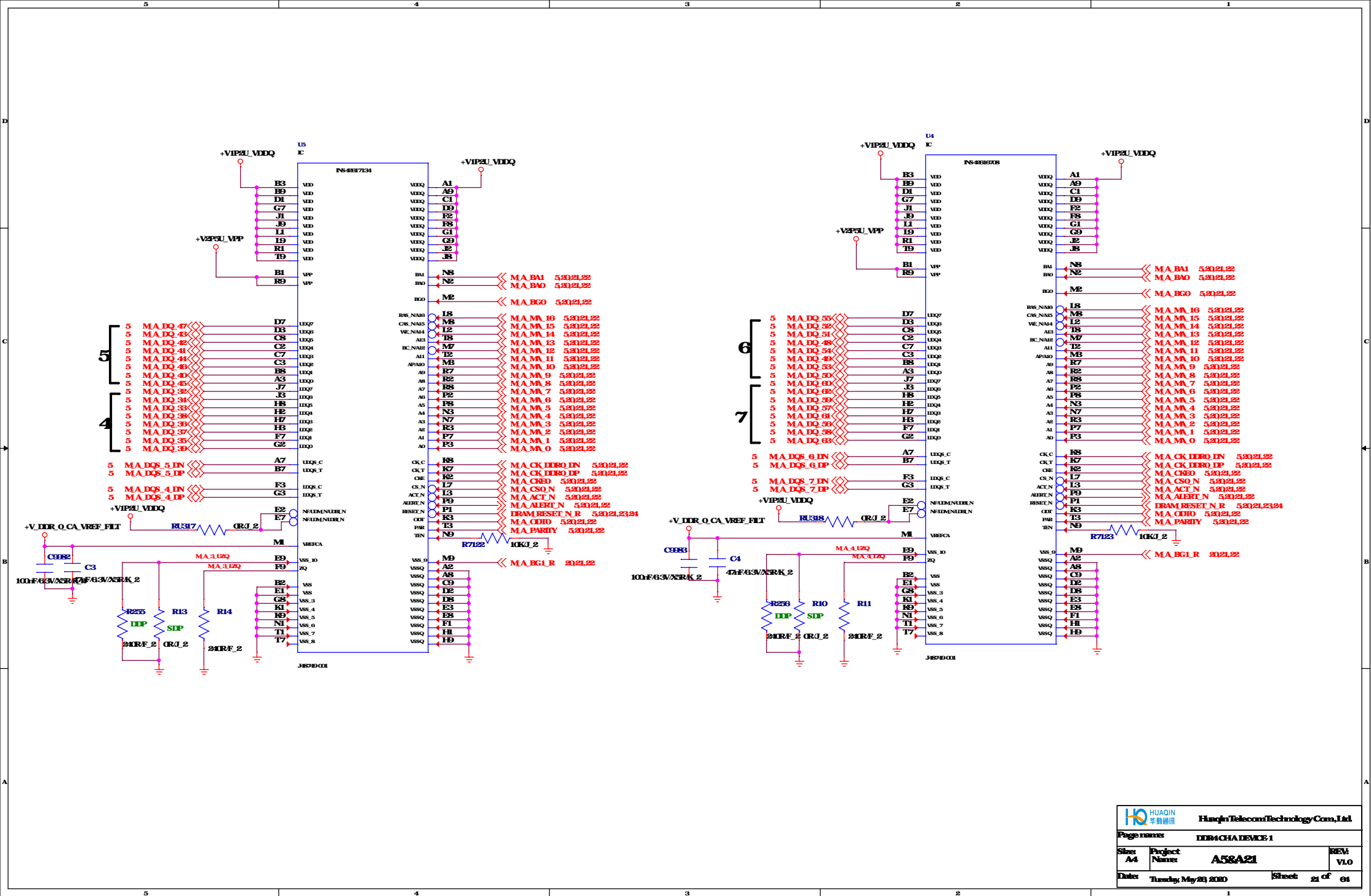
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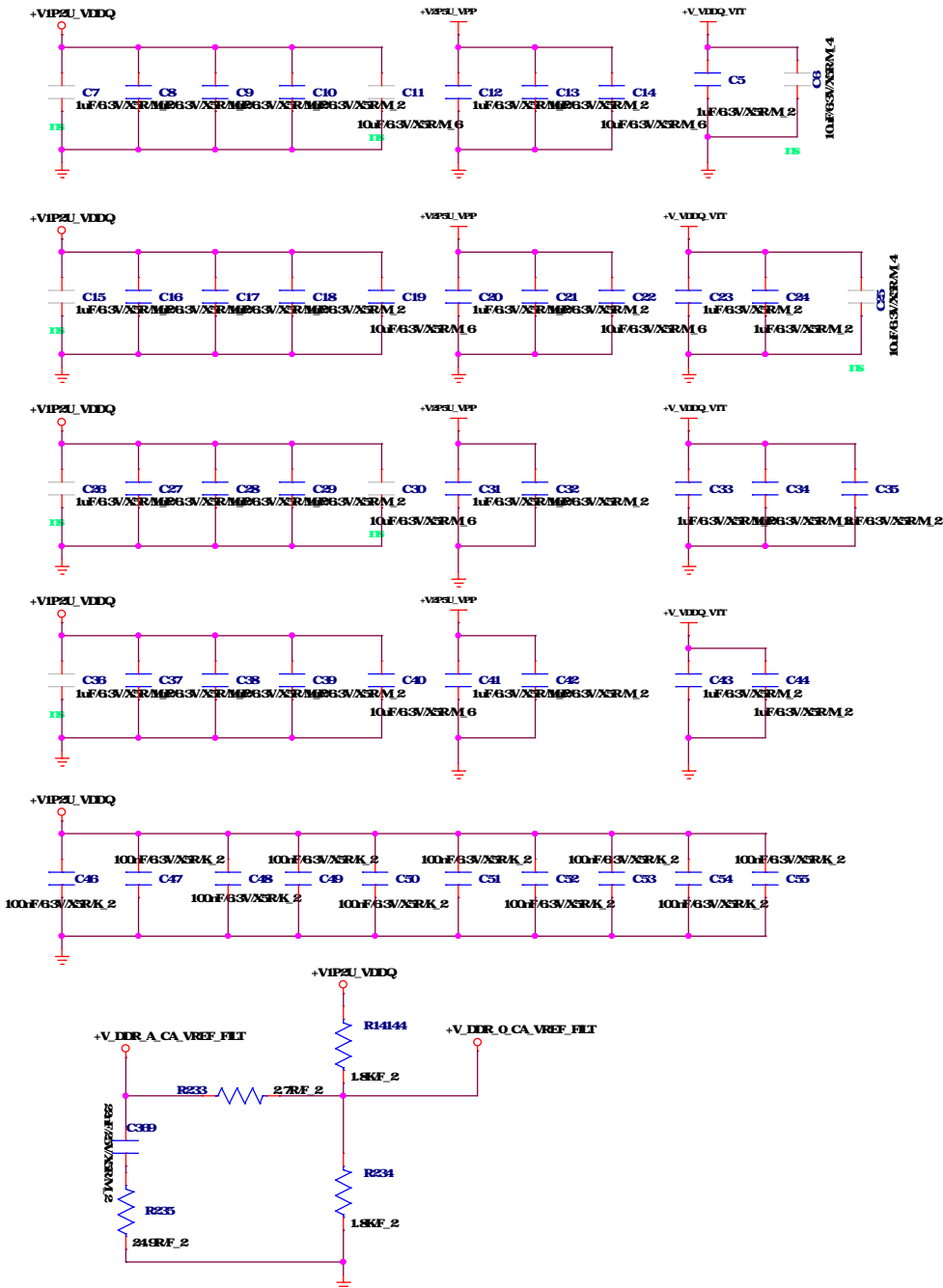




DDR PINS		SDP	DDP
EB	U2Q	GND	240EPD
MD	EG1	GND	EG1 SIG FROM CONTROLLER

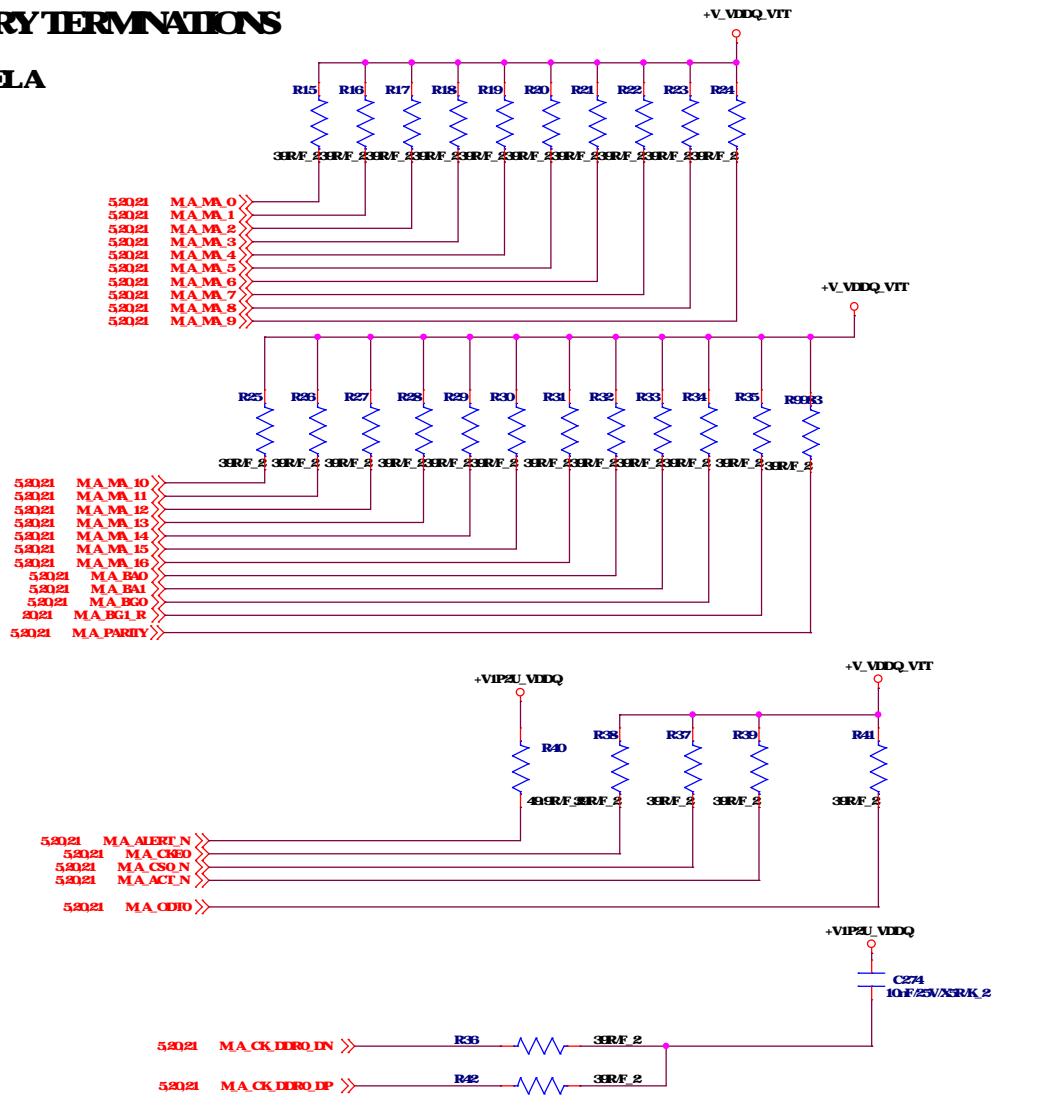



DECOUPLING CAPACITORS FOR DDR CHANNELA

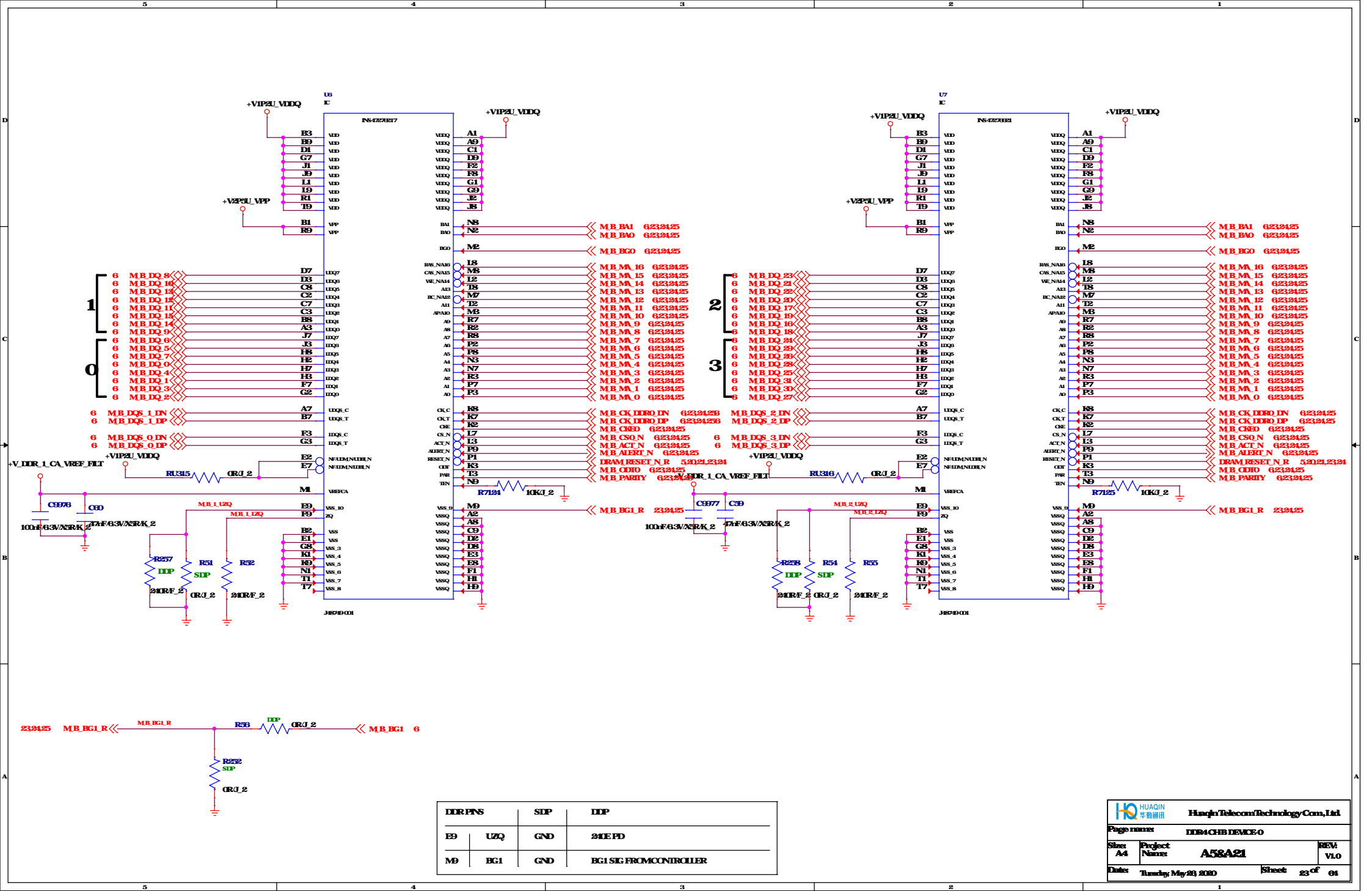


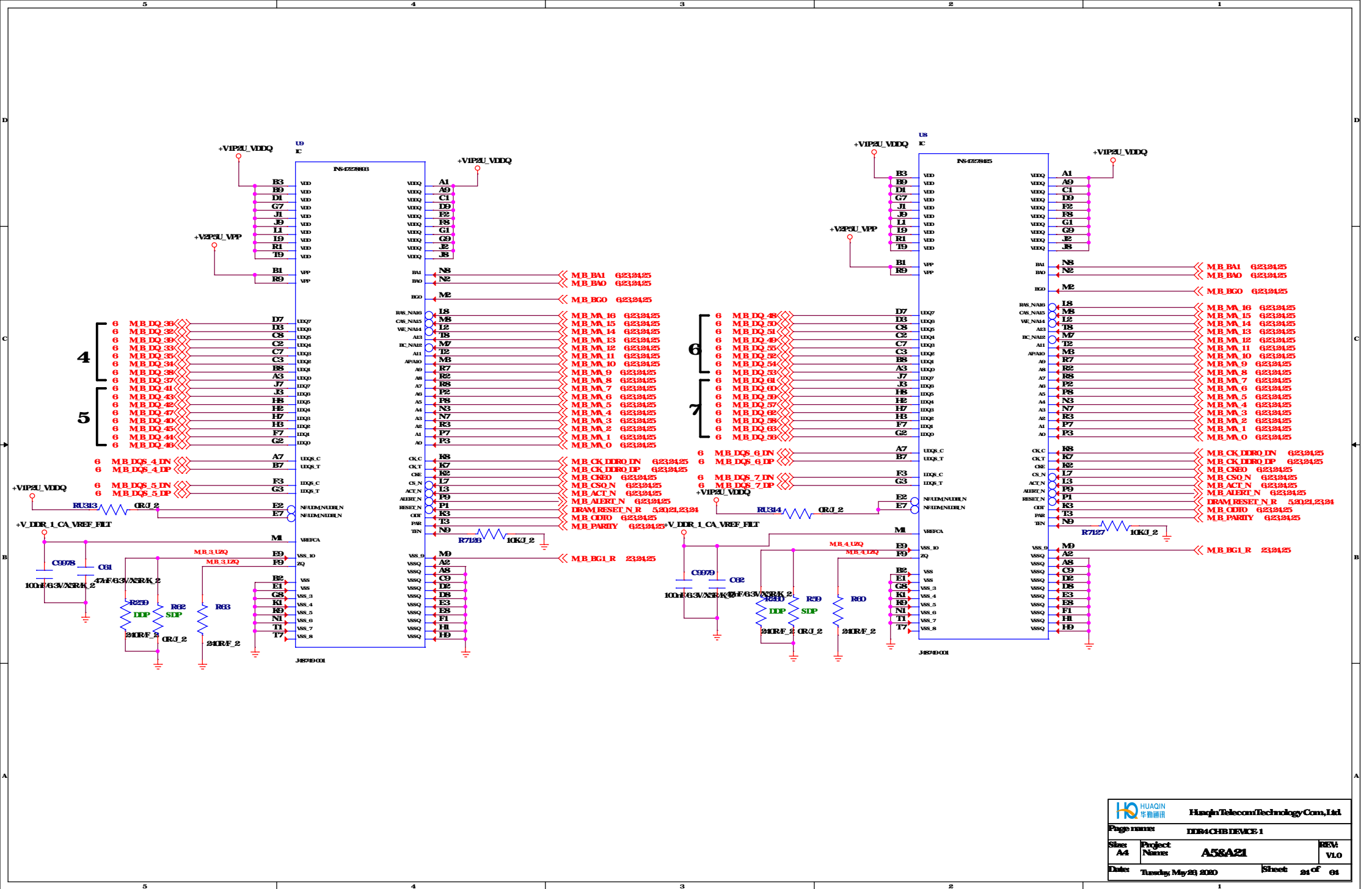
MEMORY TERMINATIONS

CHANNELA



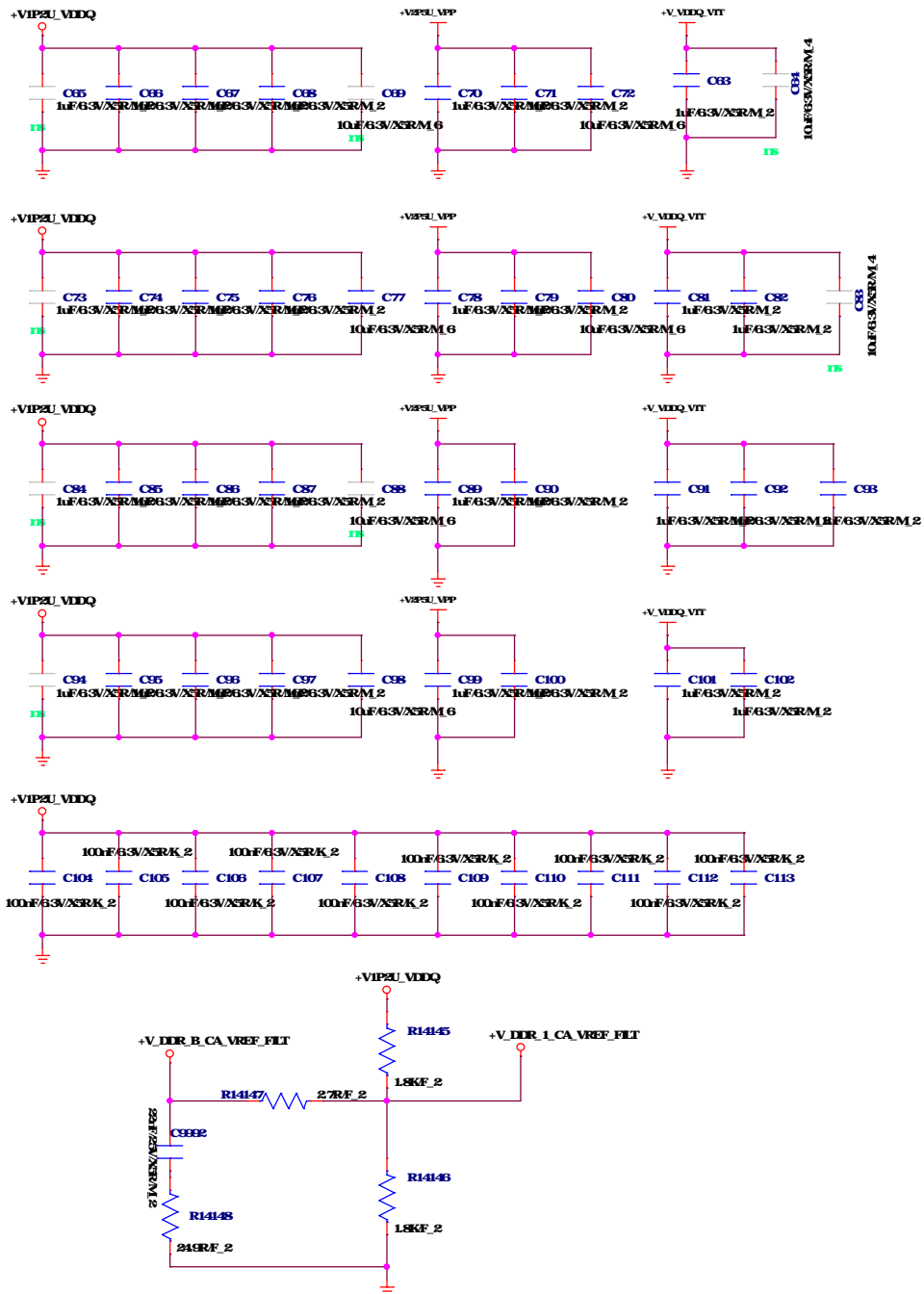
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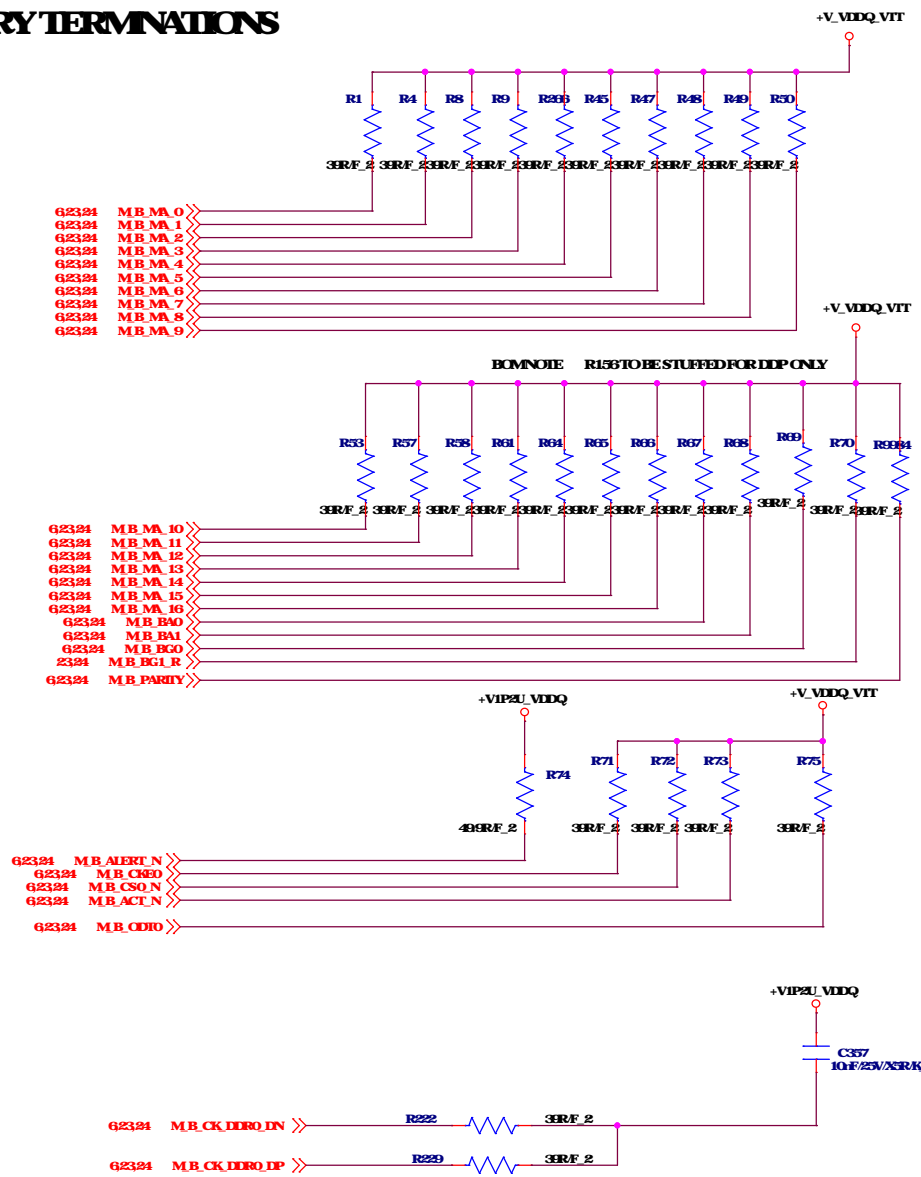


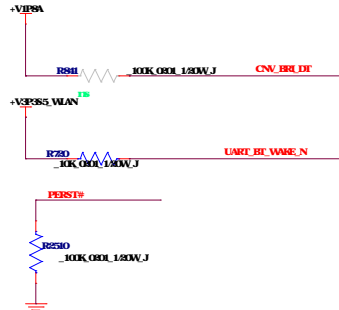
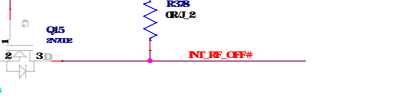
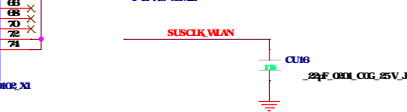
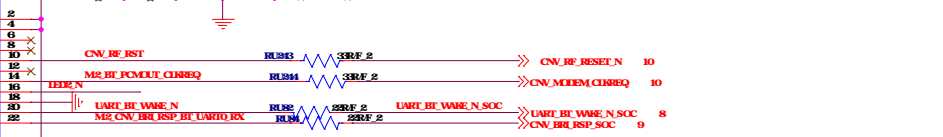
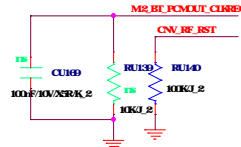
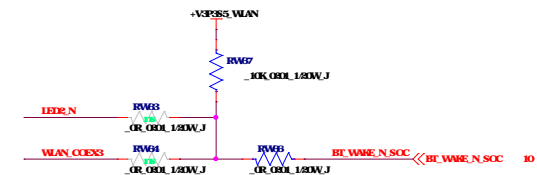


## DECOUPLING CAPACITORS FOR DDR CHANNELA

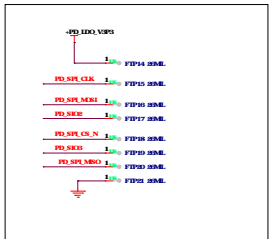
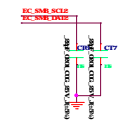
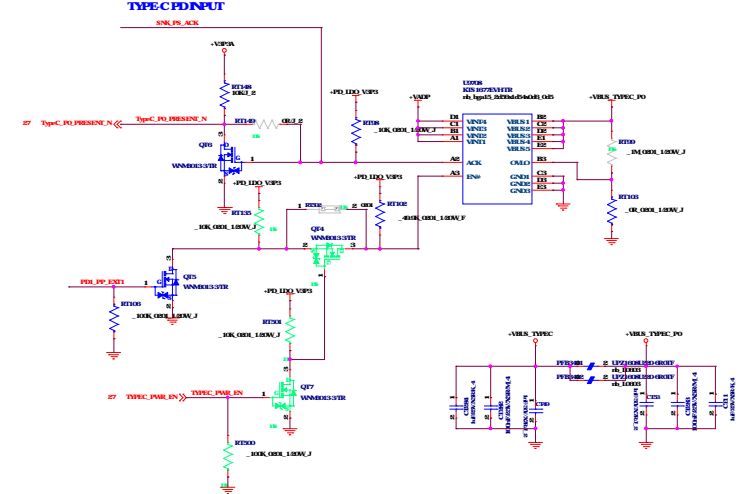


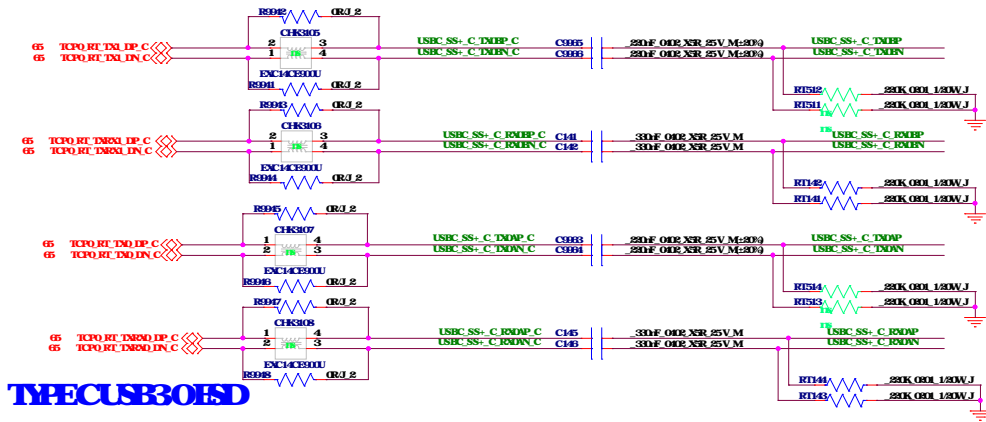
## MEMORY TERMINATIONS



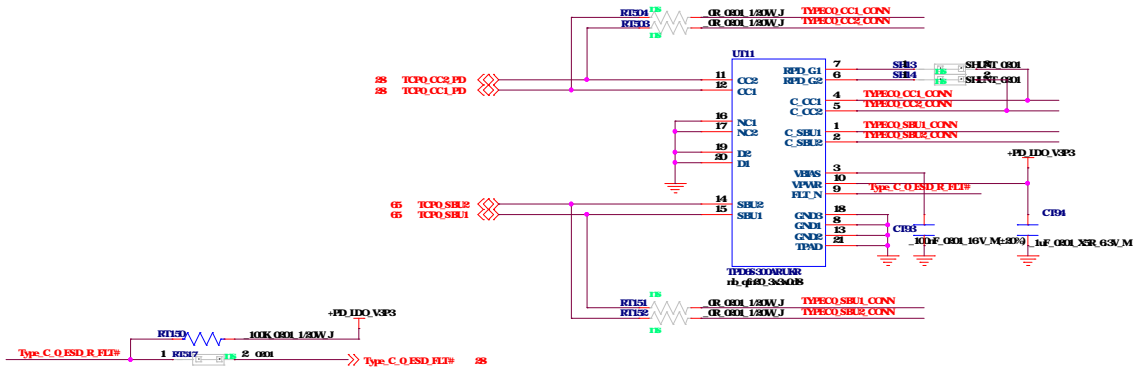
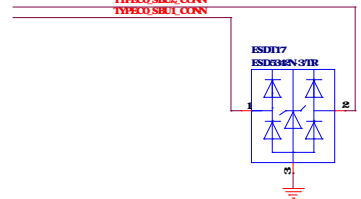
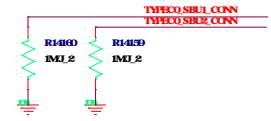
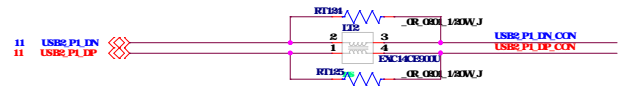
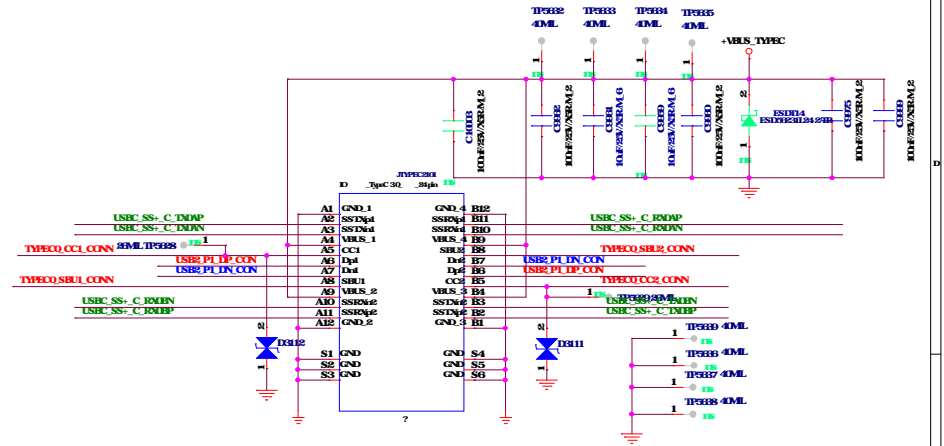
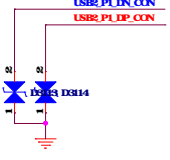
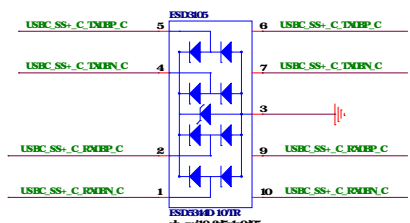
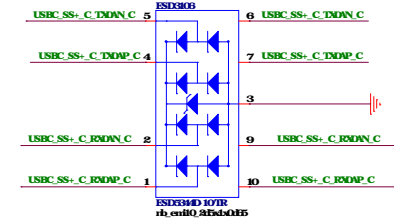




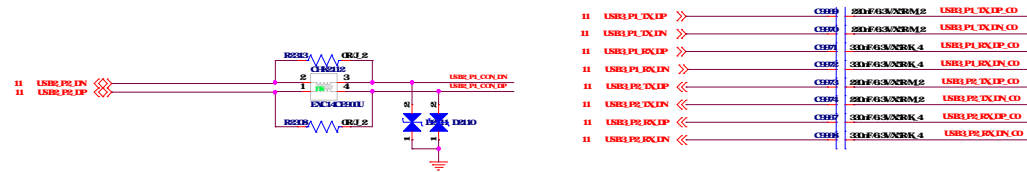




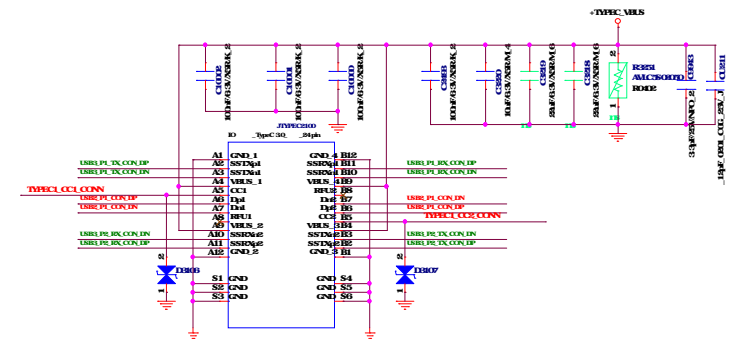
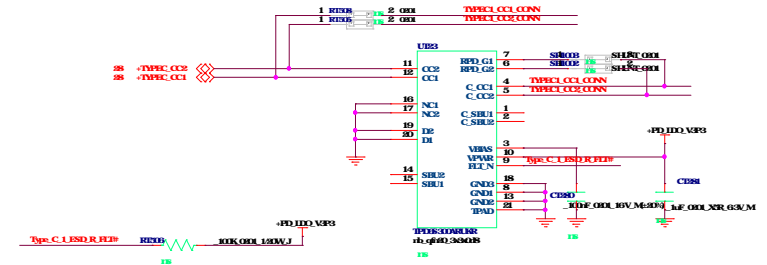
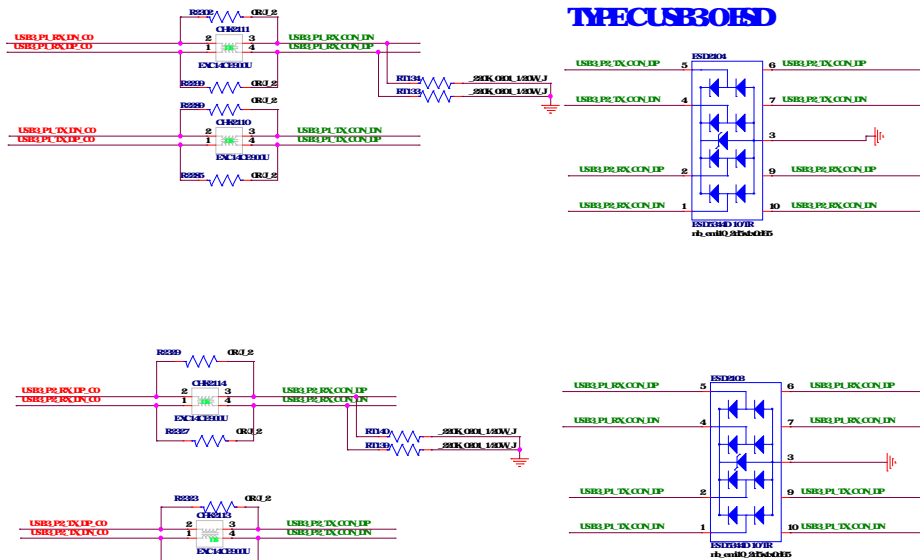
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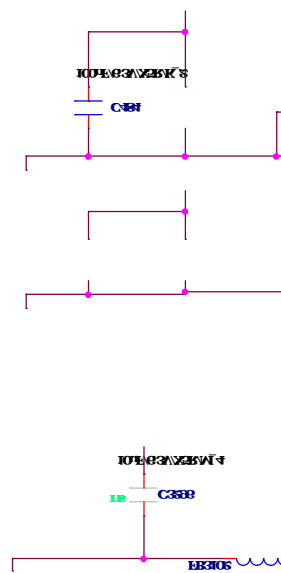
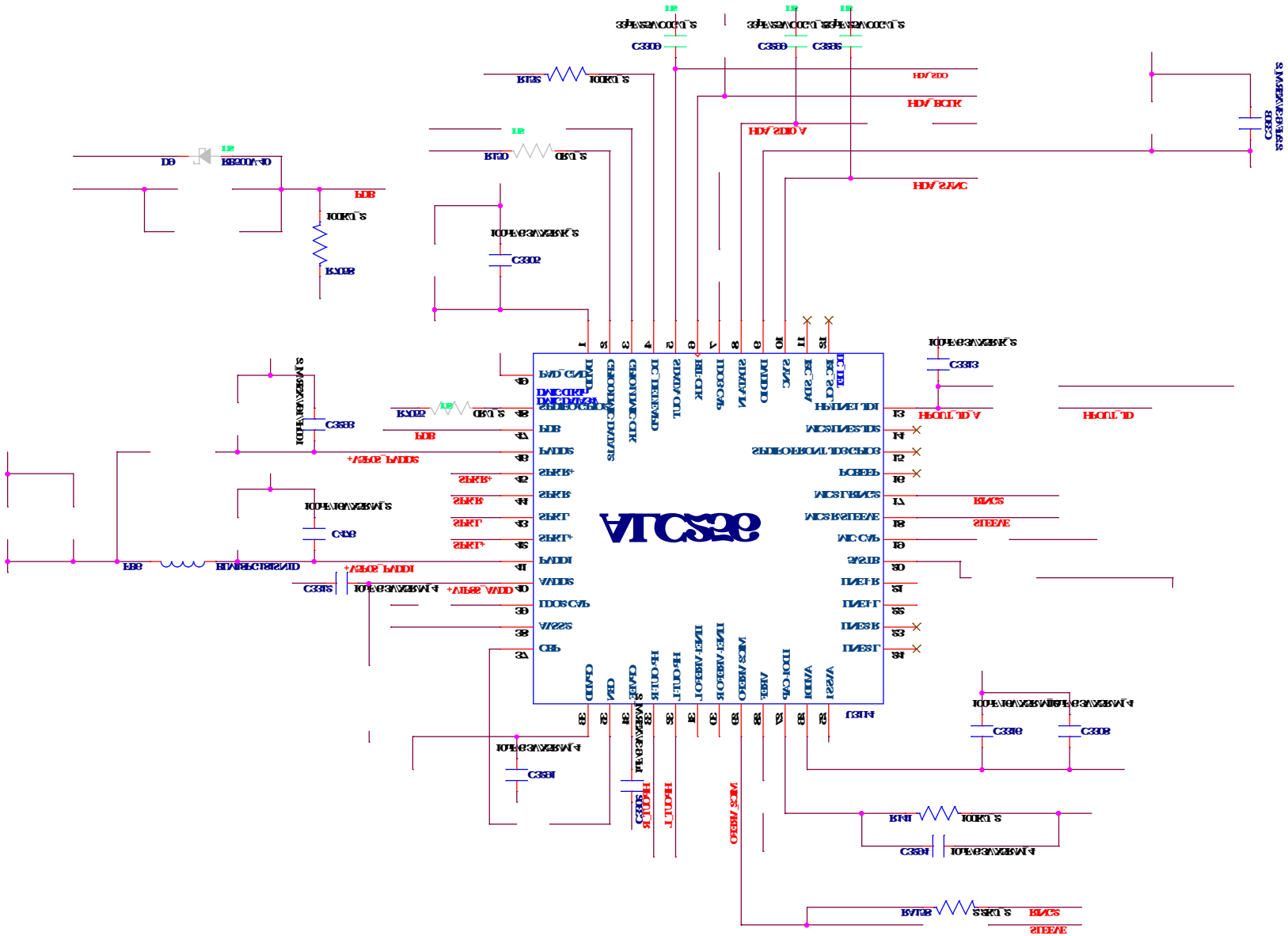
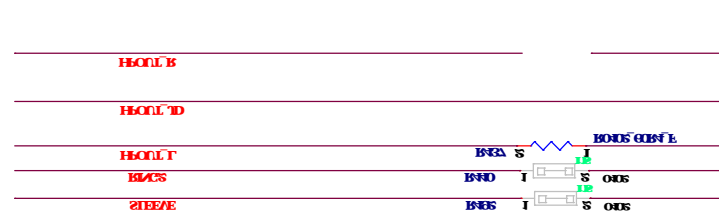
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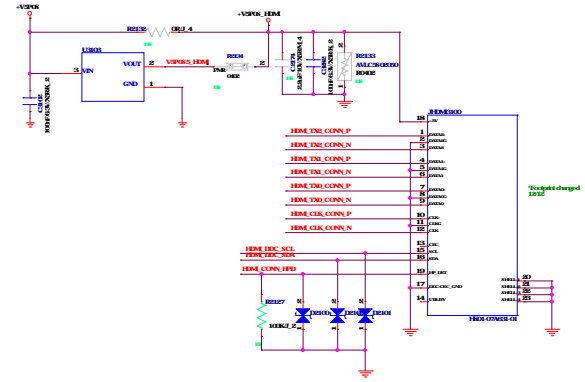
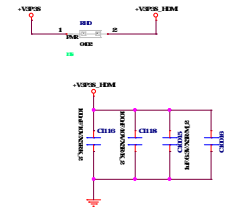
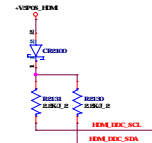
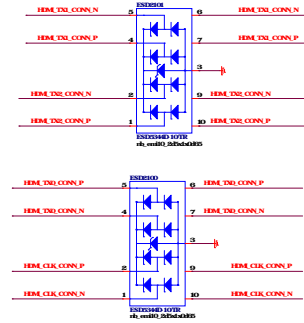
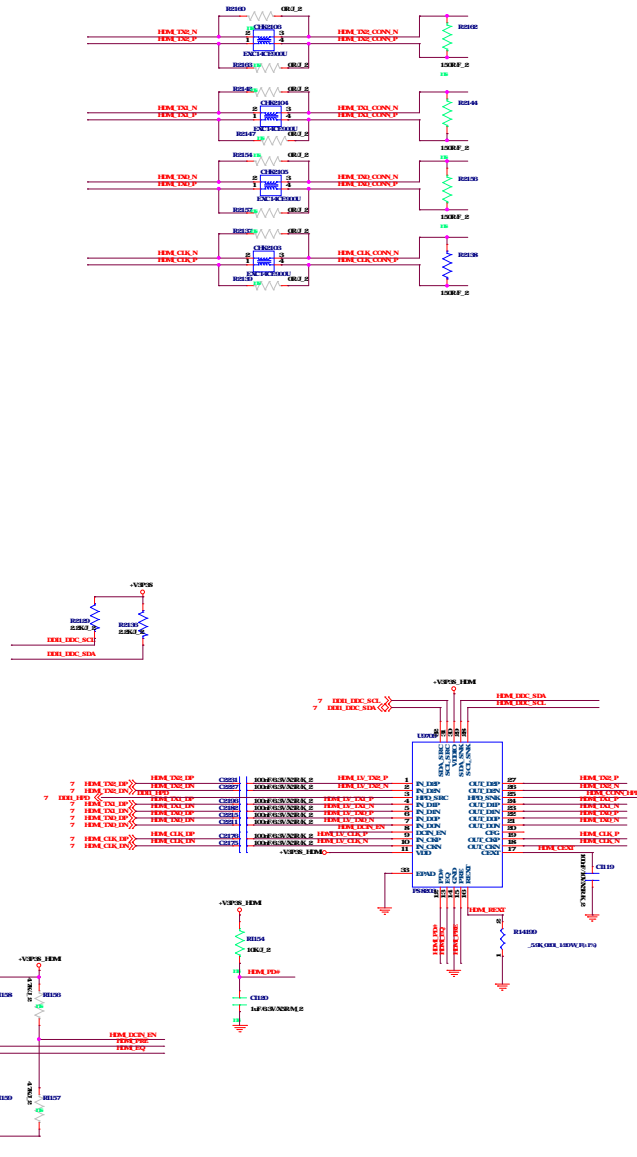


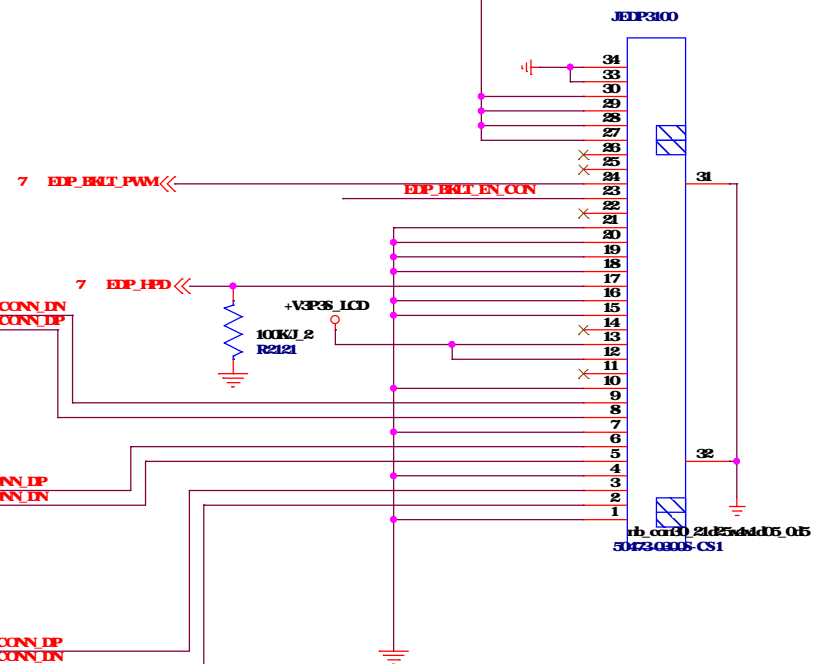
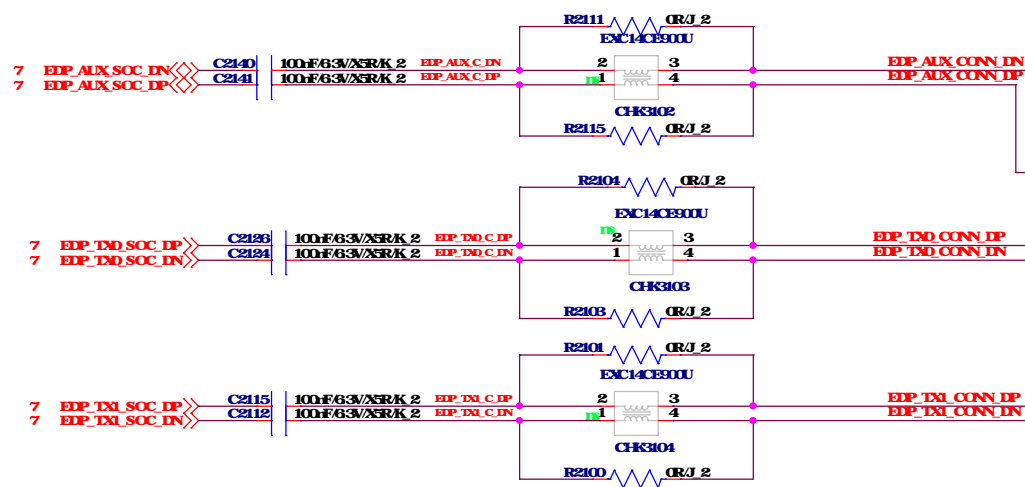
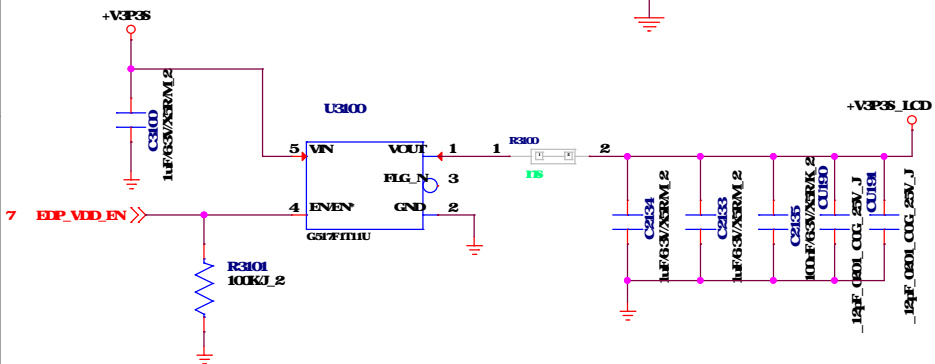
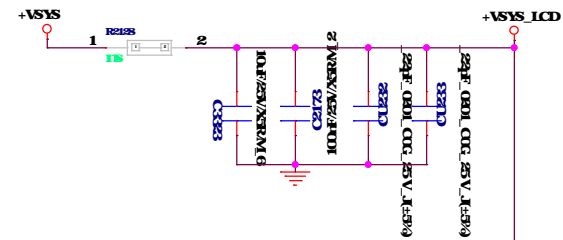




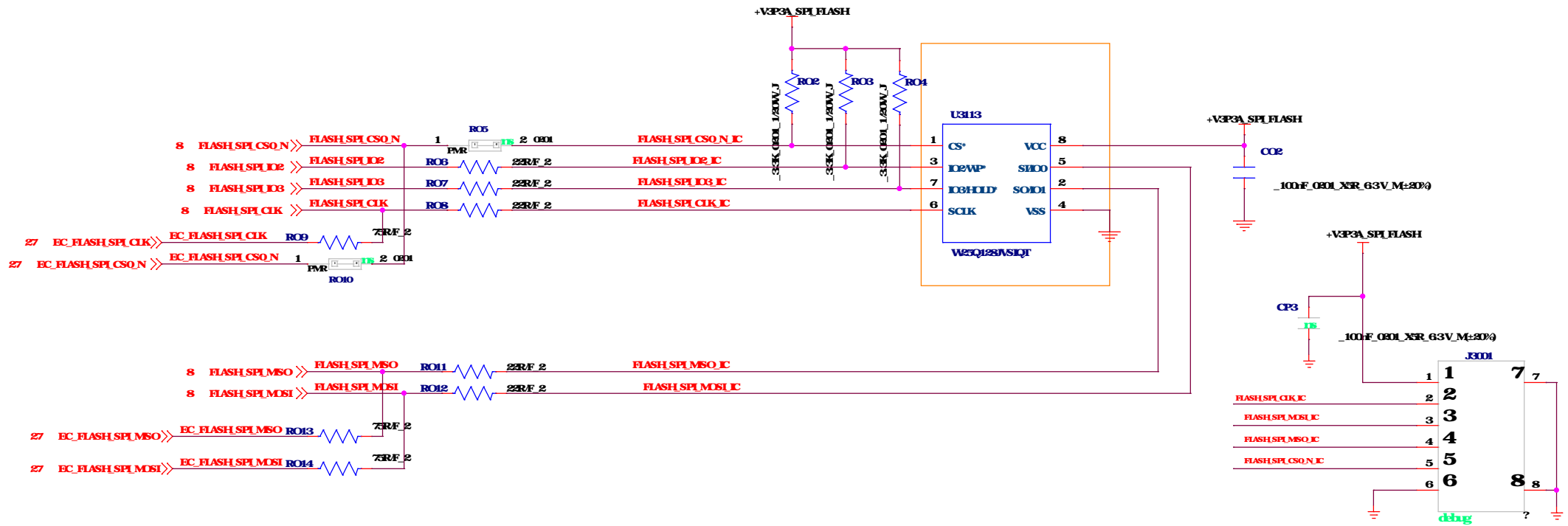
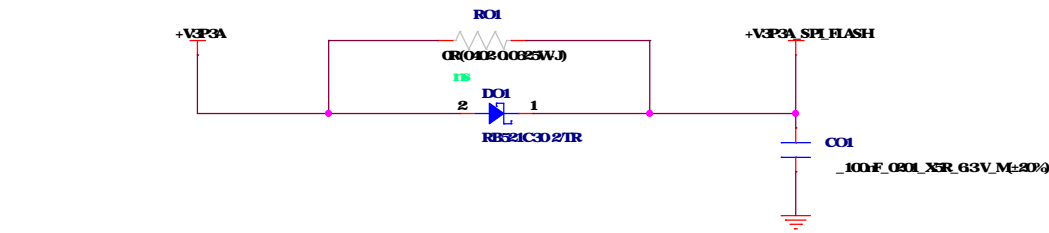
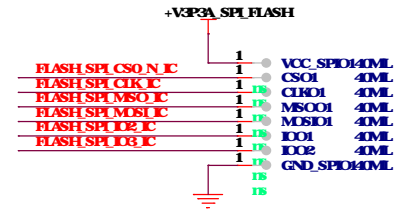


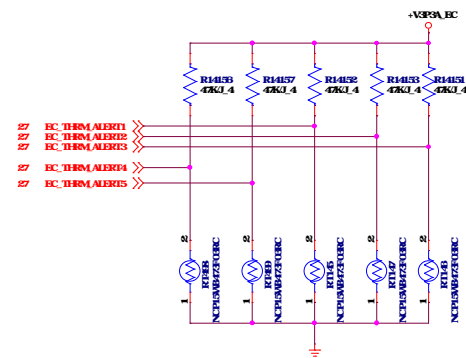
# HDMI4

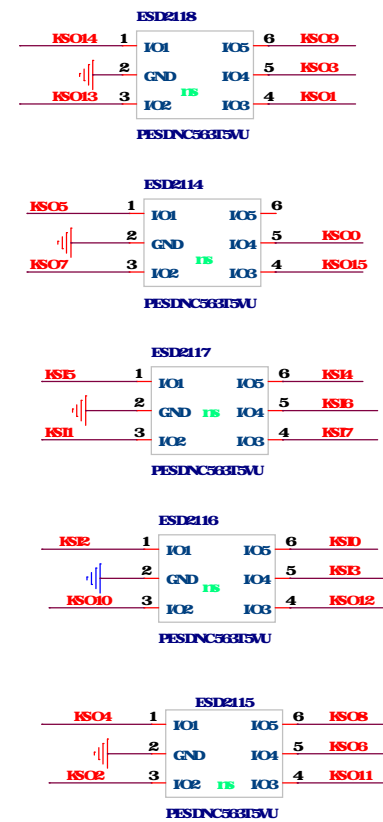




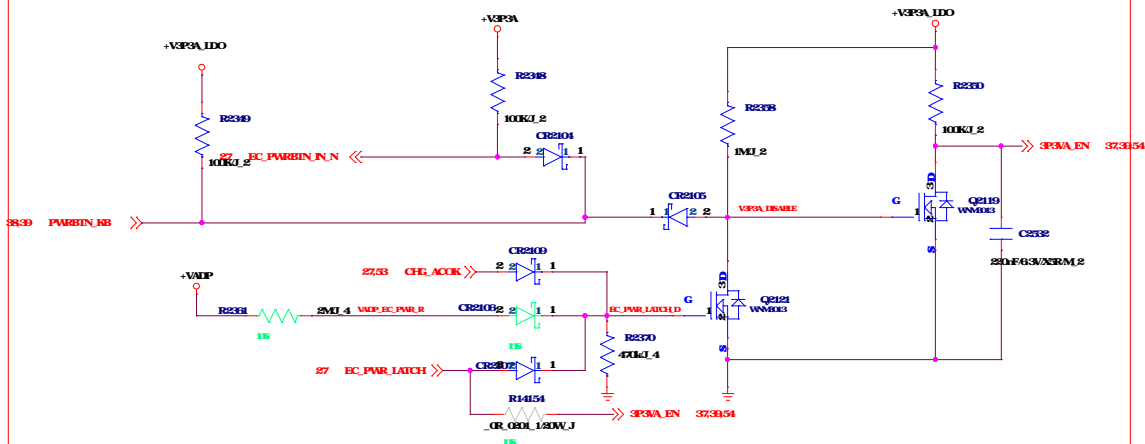
# FOR product line



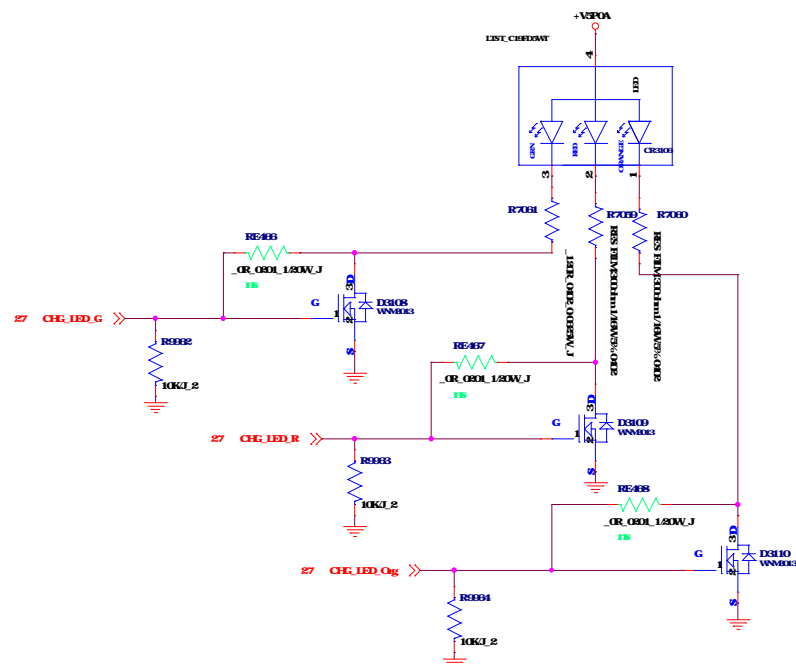
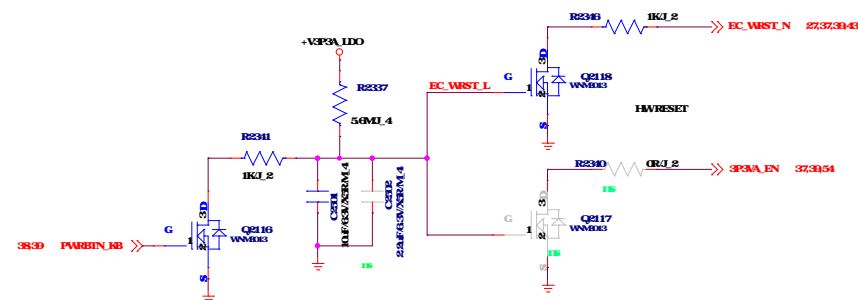




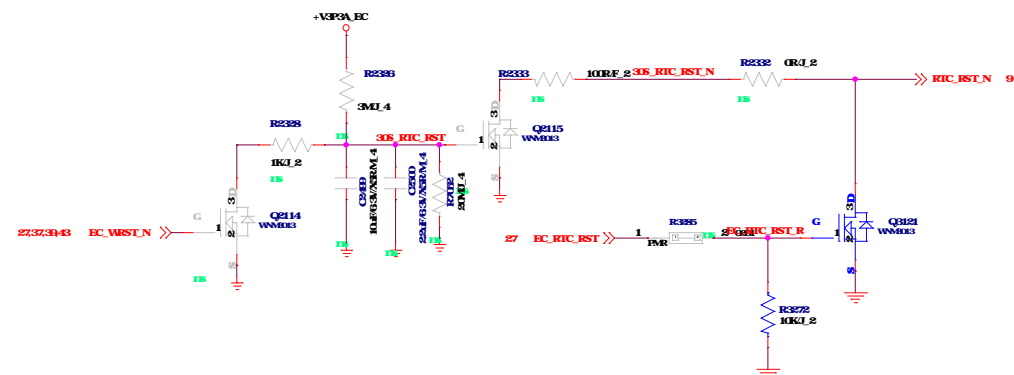
## PVR ON LOGIC



## 158 Force Power Down



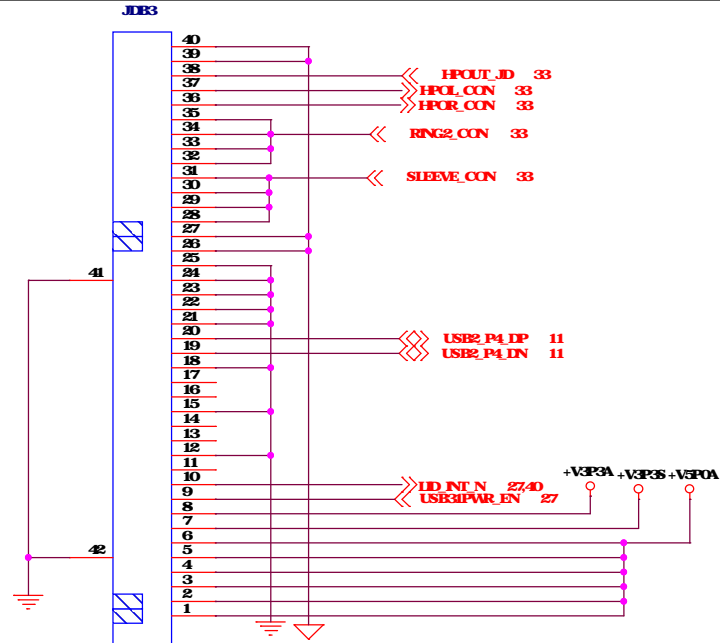
### 30S RTC RESET





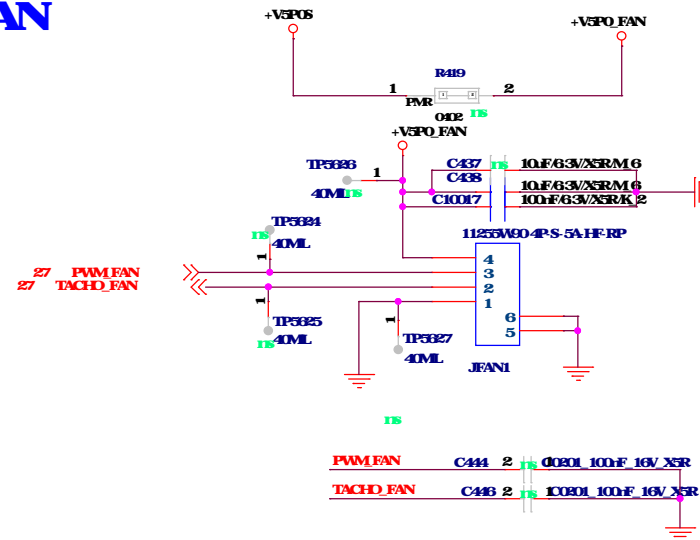


# DB

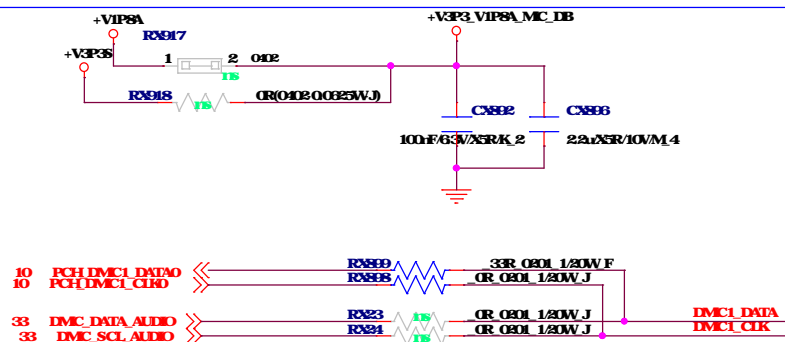


rh.com10 23Bd4Bd5  
ARC34S41P6A1Z

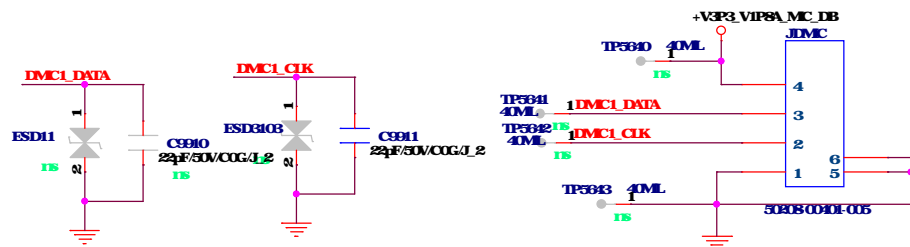
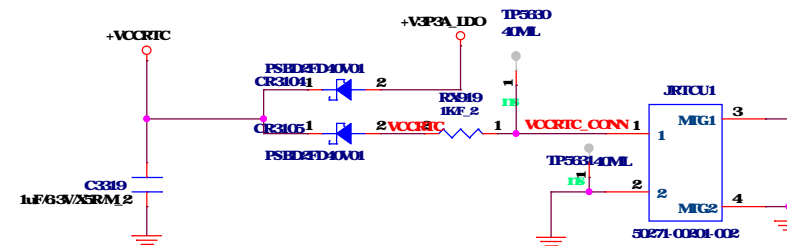
# FAN



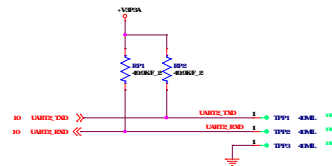
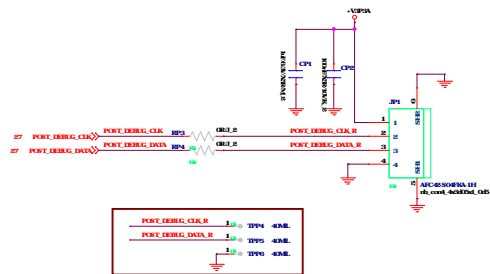
# DMC



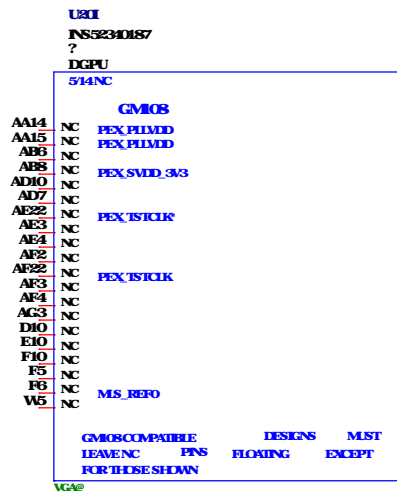
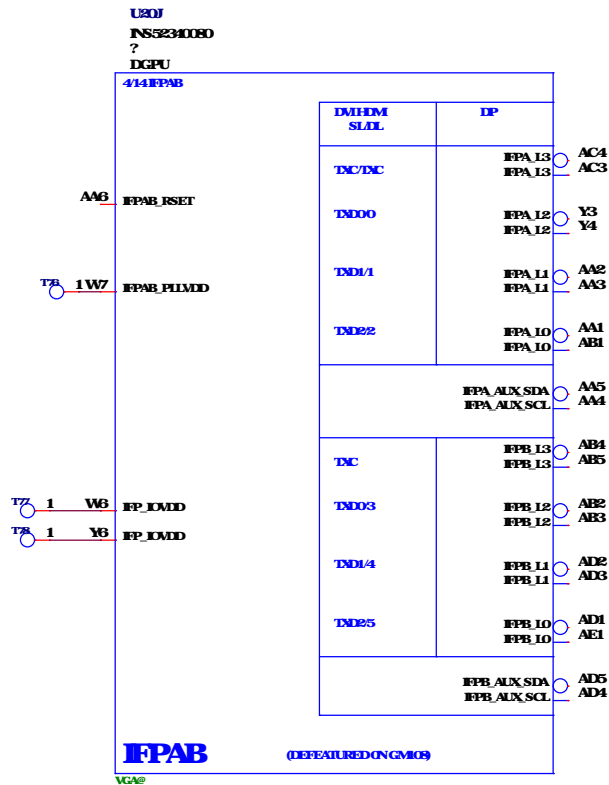
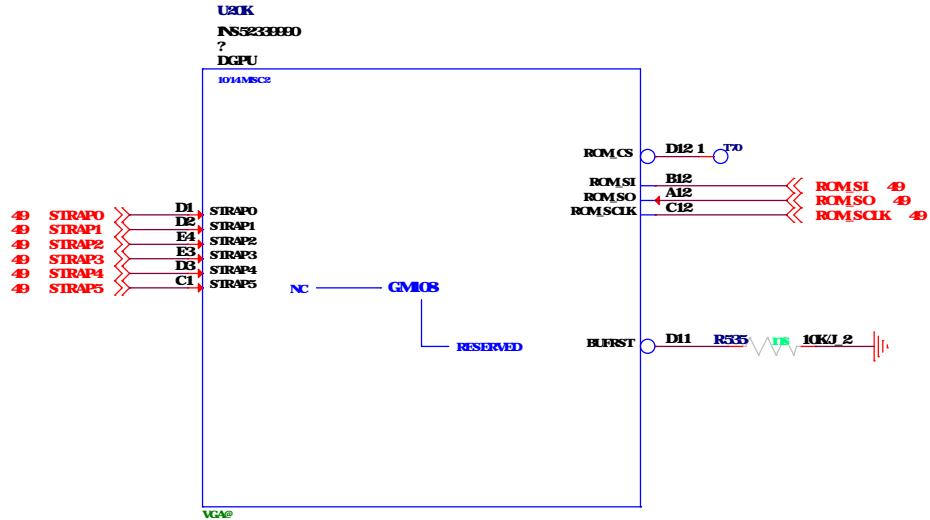
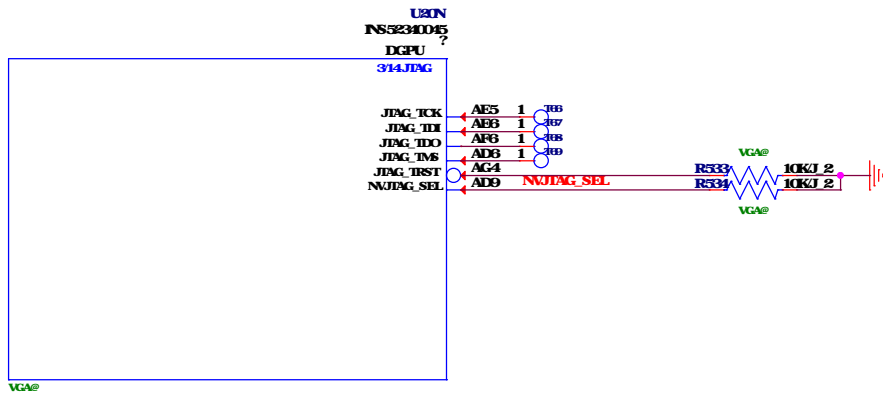
# RTC



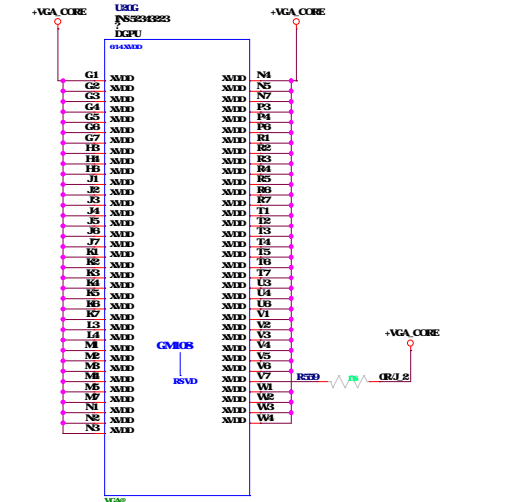
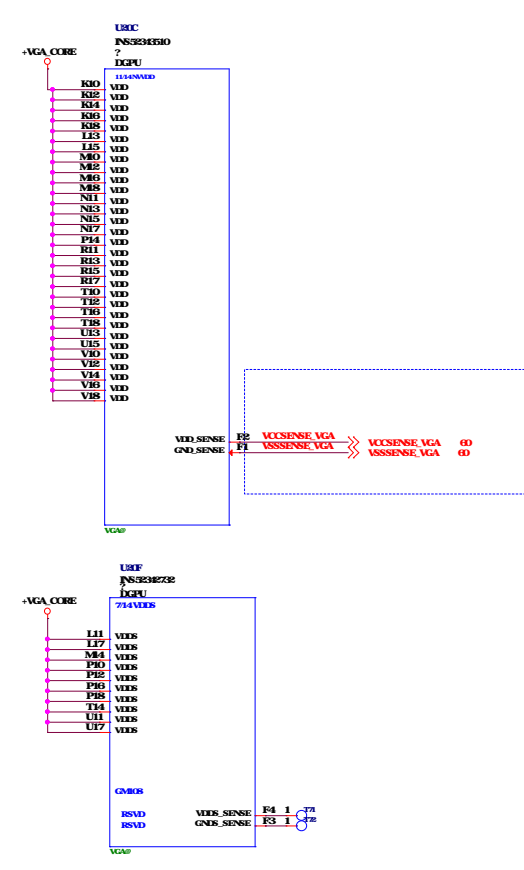
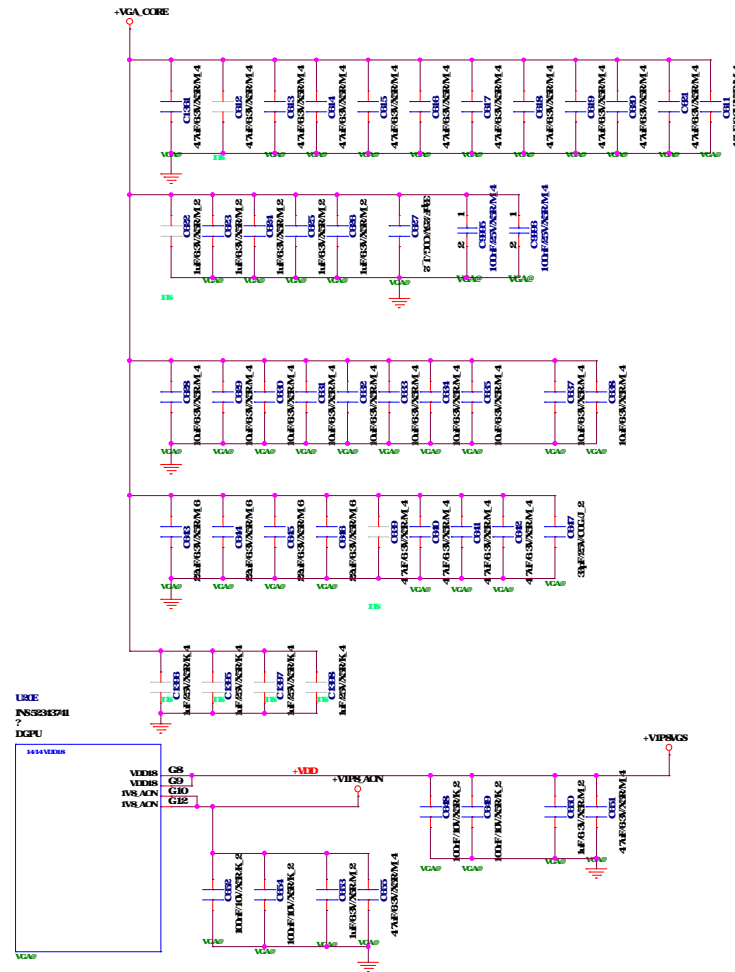
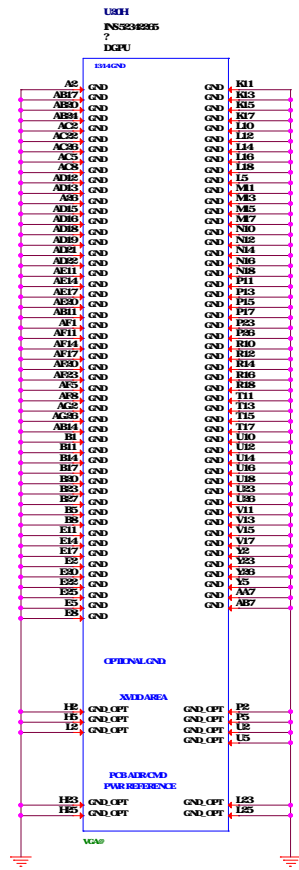
HUAQIN 华勤通信		Huaqin Telecom Technology Co., Ltd.	
Page name:		DBMC/FAN/RTC	
Size: A4	Project Name:	A58A21	REV: V1.0
Date:	Tuesday, May 23, 2020	Sheet:	41 of 61





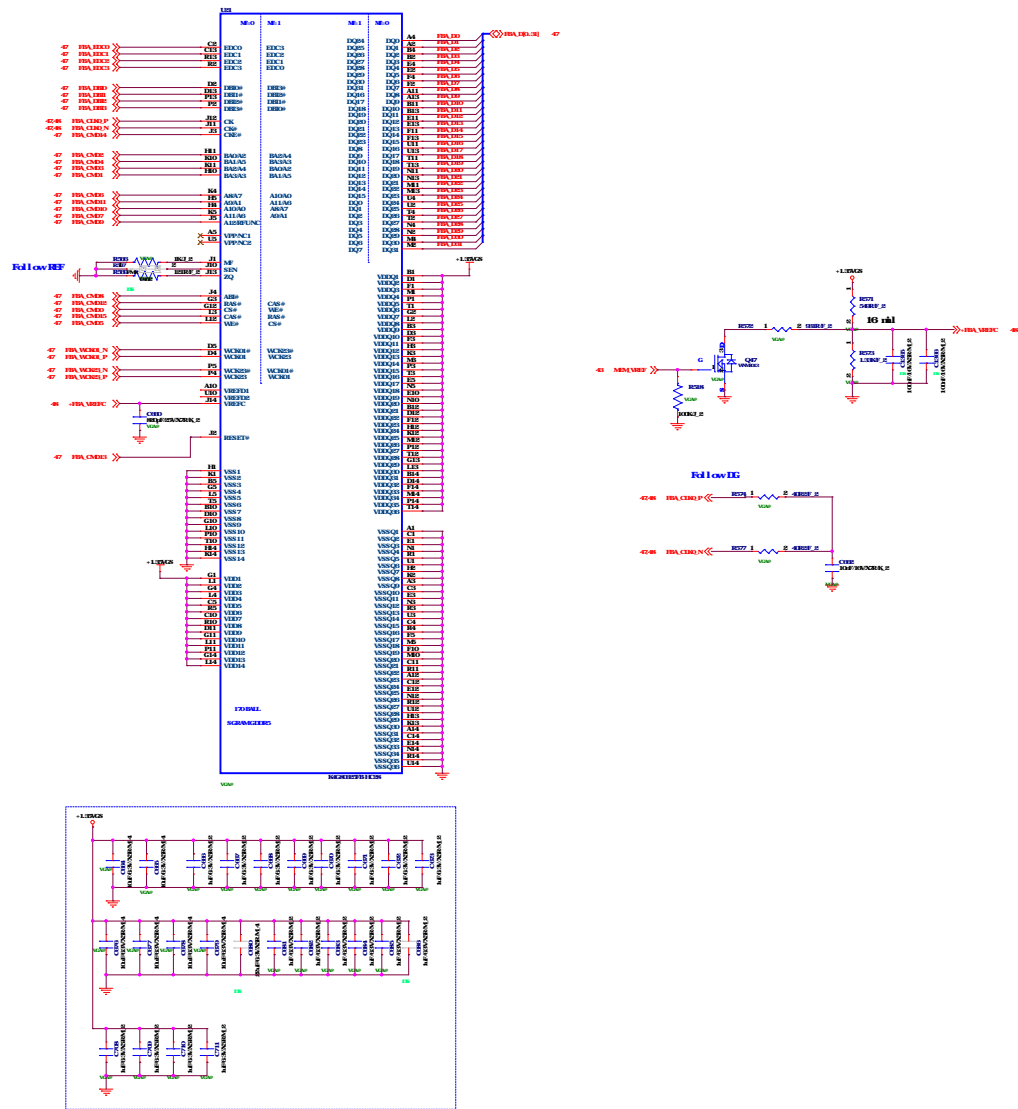




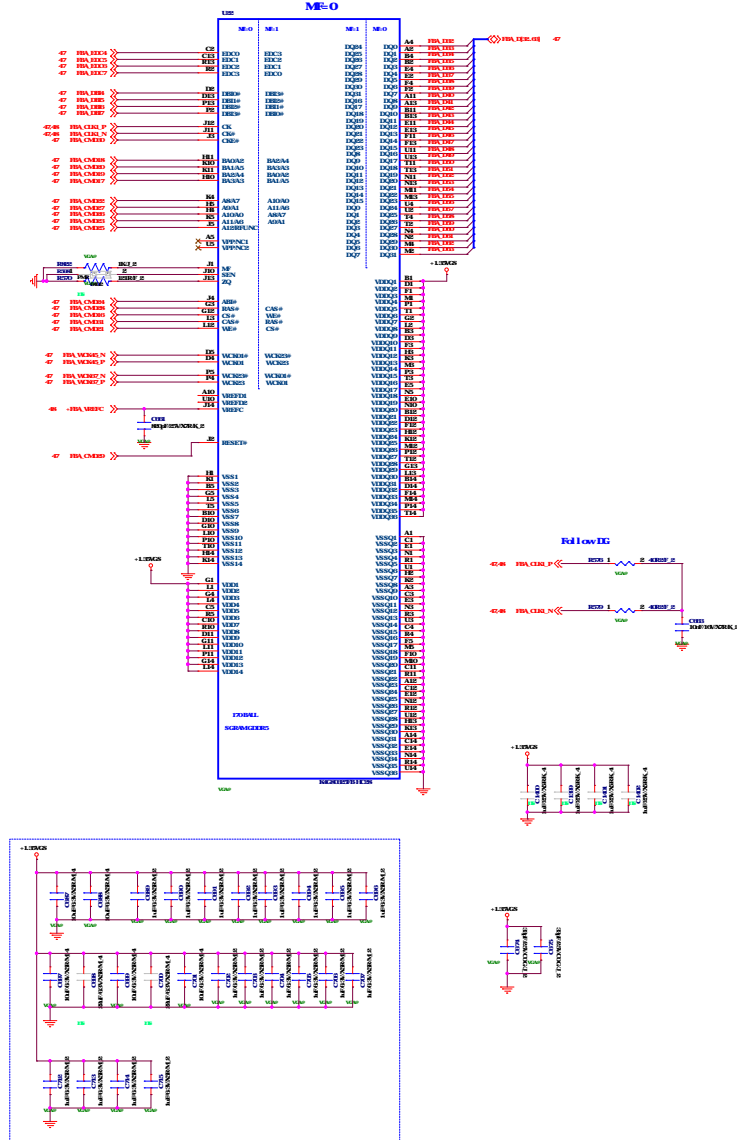




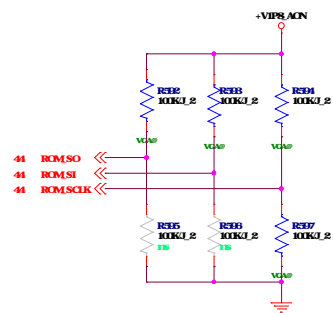
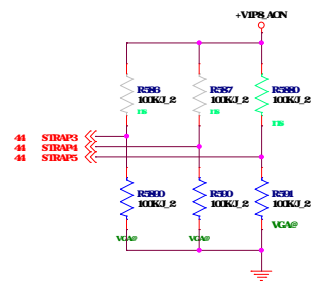
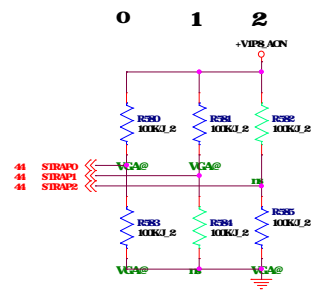
## Memory - Lower 32 bits



## Memory - Upper 32 bits







SMBUS_ALT_ADDR	
0	0x0E (Default)
1	0x0C (Mini-GPU usage)

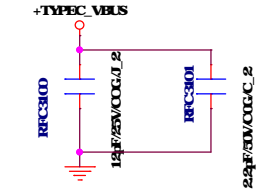
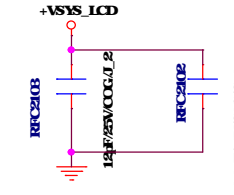
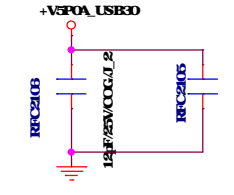
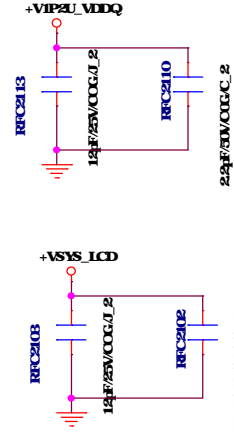
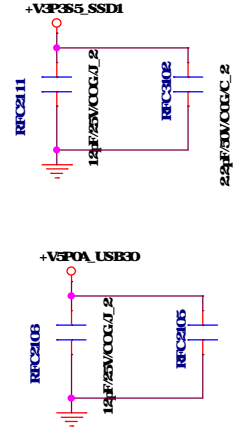
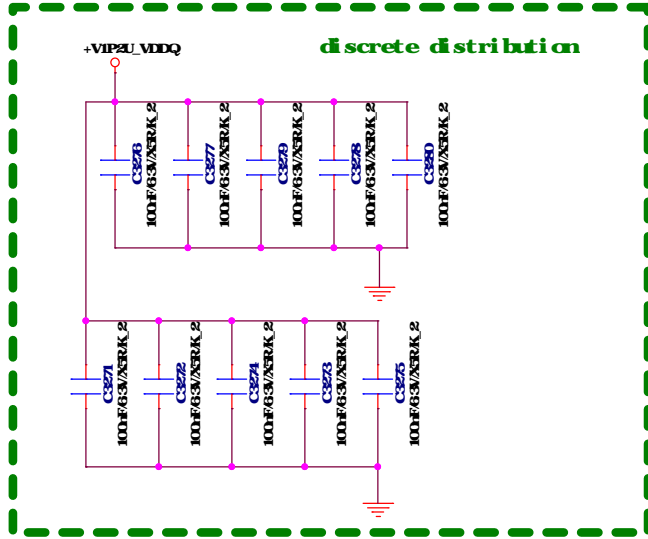
DEVID_SEL	
0	(Default)
1	

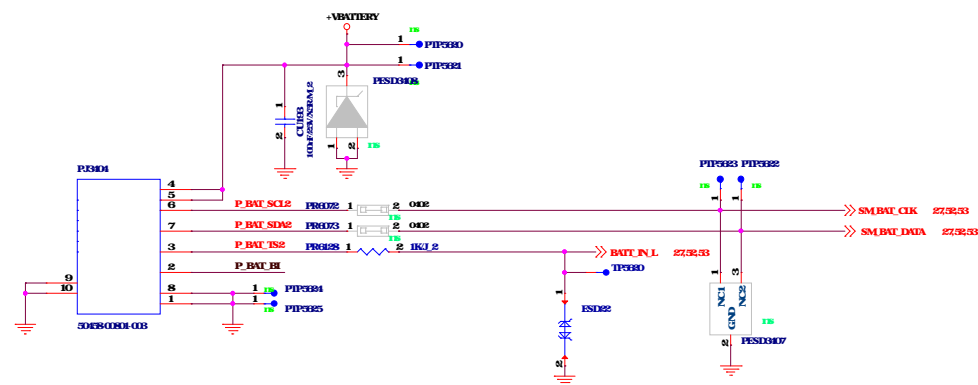
PCI_CFG	
0	(Default)
1	

VGA_DEVICE	
0	3D Device (Class Code 303F)
1	VGA Device (Default)

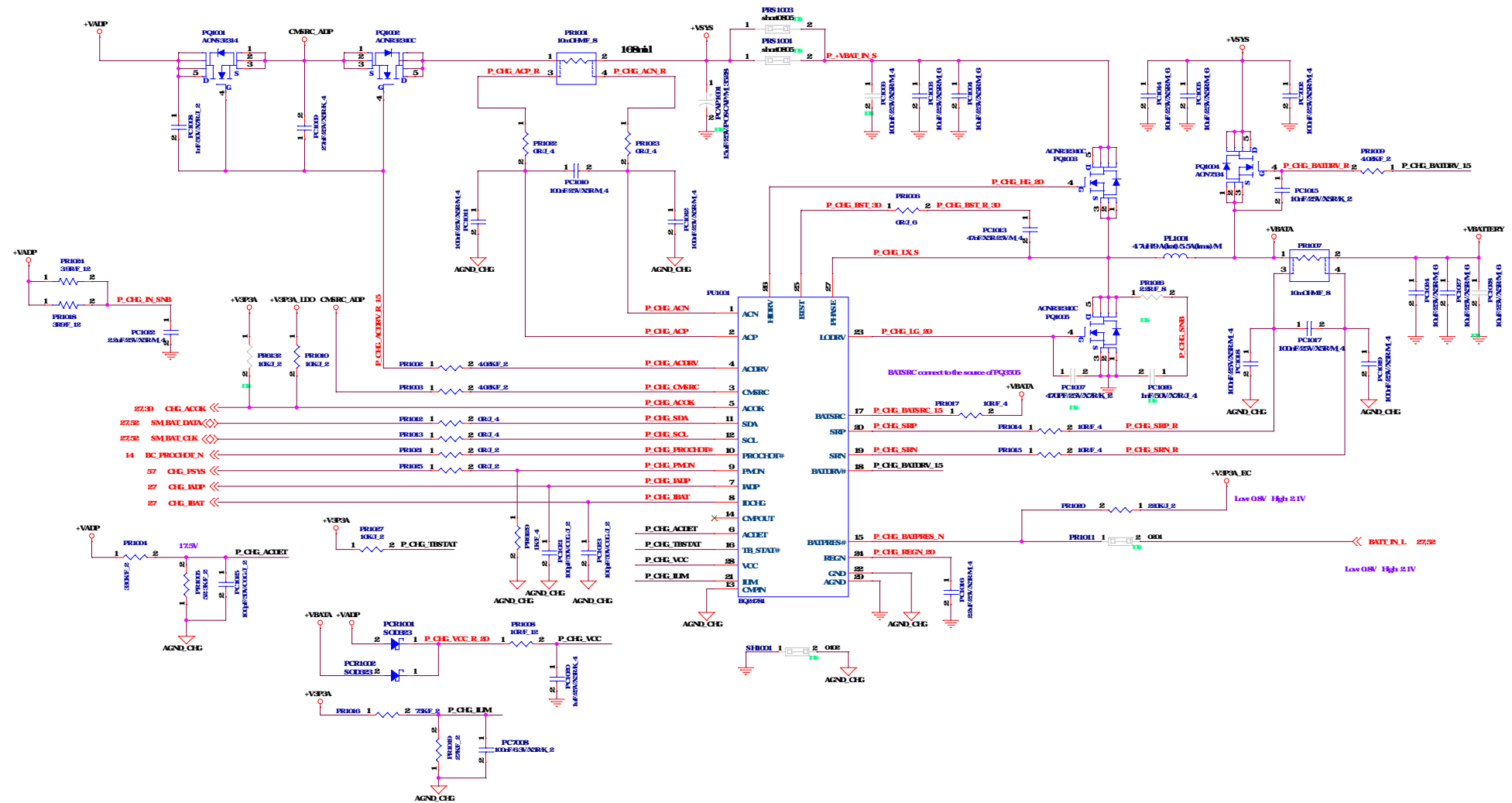
Physical Strapping pin	Power Rail	SCR3_EXPOSED	SCR2_EXPOSED	SCR1_EXPOSED	SCR0_EXPOSED
ROMSCLK	M	Disable	Disable	Disable	Disable
ROMSI	H				
ROMSO	H				

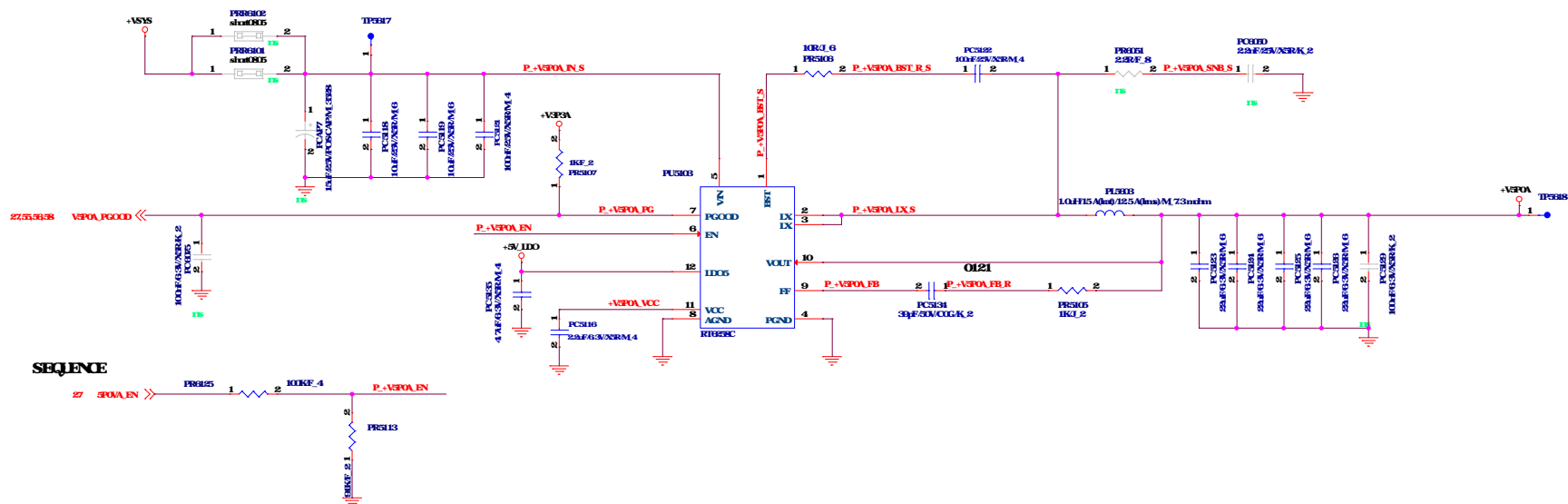




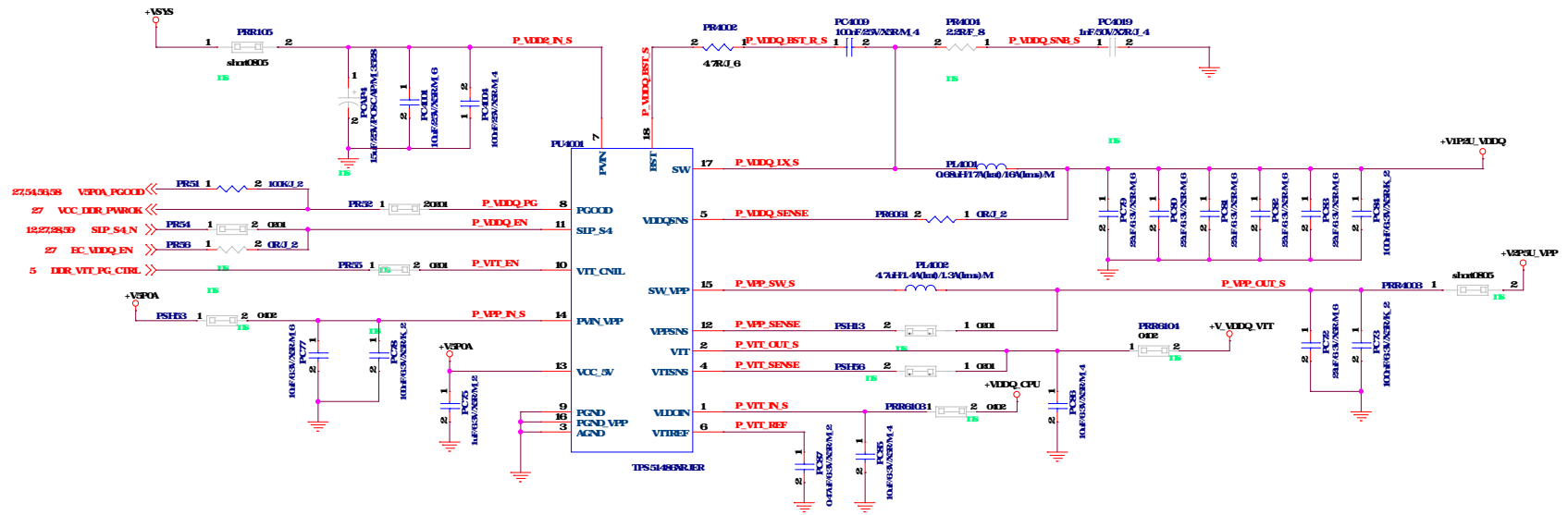
[illegible]

## SystemCharger[BQ24781]





## SEQUENCE









# +VIP8A

